

X570 UD

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2015.12.30~B.L

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Title

COVER SHEET

Size

Custom

Document Number

X570 UD

Rev

1.0

Date:

Monday, June 24, 2019

Sheet

1

of

47

[illegible][illegible][illegible][illegible]

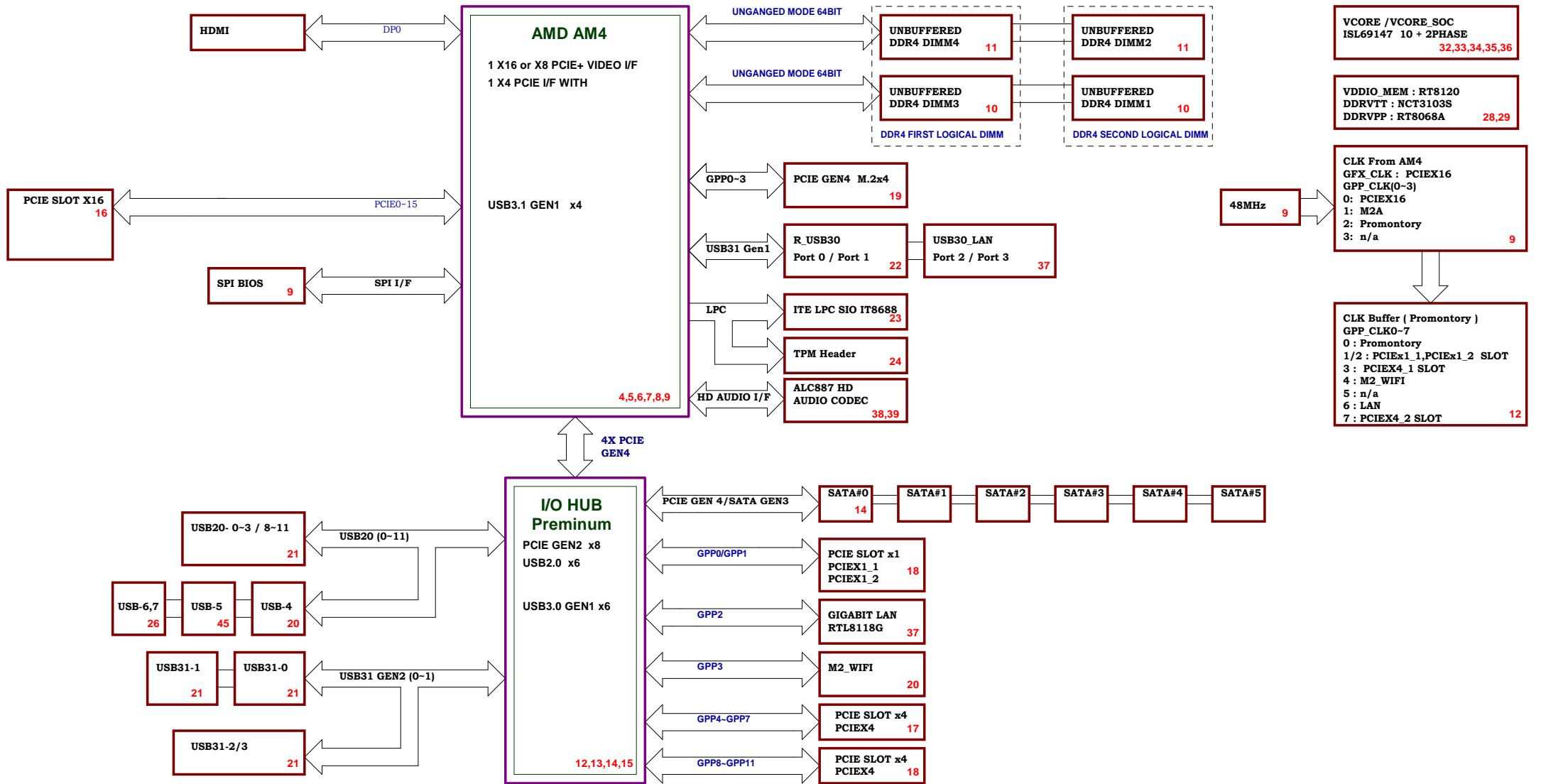
Model Name:X570 UD

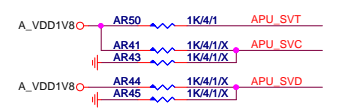
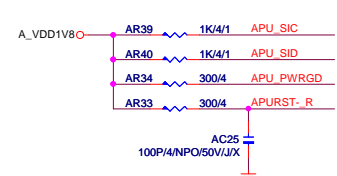
Component value change history

Version: 1.0
P-Code: U98126-0

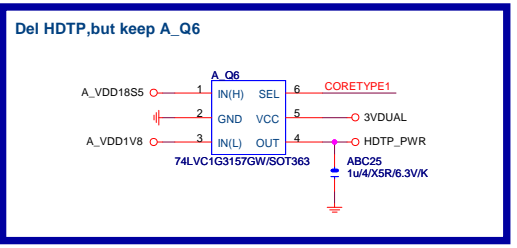
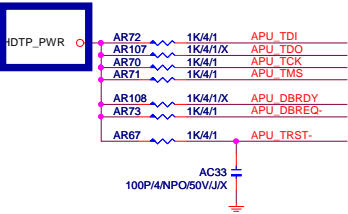
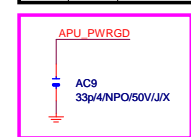
Date	Change Item	Reason
2019/05/31	first release	
	9MX57UD-00-01 BOM	
2019/07/09	9MX57UD-00-10A BOM	
	1.QFR8->X,QFR17 上件 2.PM_HS->12SP2-S11013-21R / 22R	
	, RMOS->12SP2-S08823-21R / 22R , TMOS->12SP2-S11233-21R / 22R	
	3.MCU1->X 4.M_BIOS Scoket->X 5.WIFI 不上件	
	6.DU1->10TA1-669147-04R,DAJP->X 7.110A->10KS2-040131-02R	

[illegible][illegible]

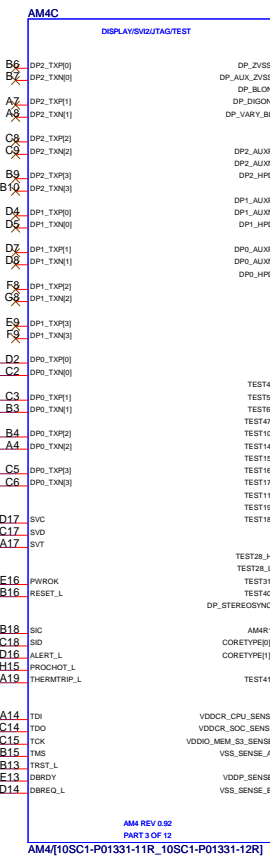
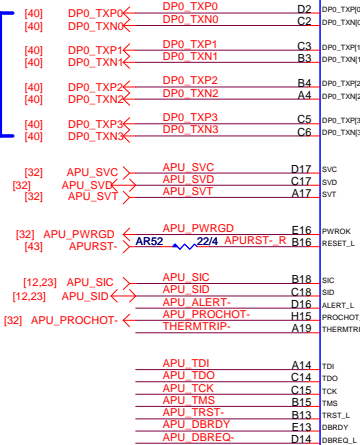




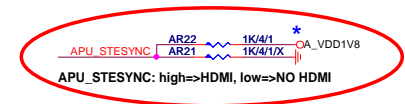
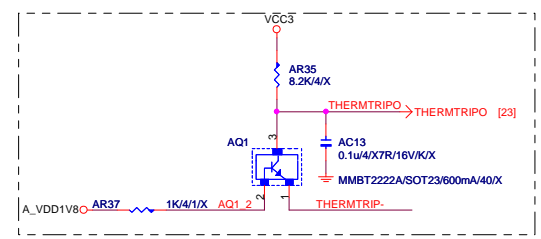
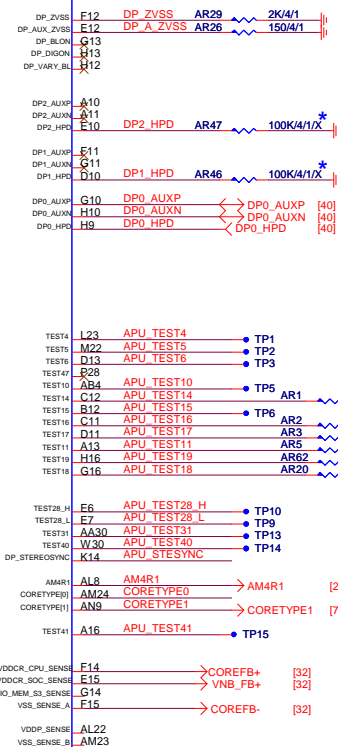
SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



HDMI



Placed within 1500 mils from APU



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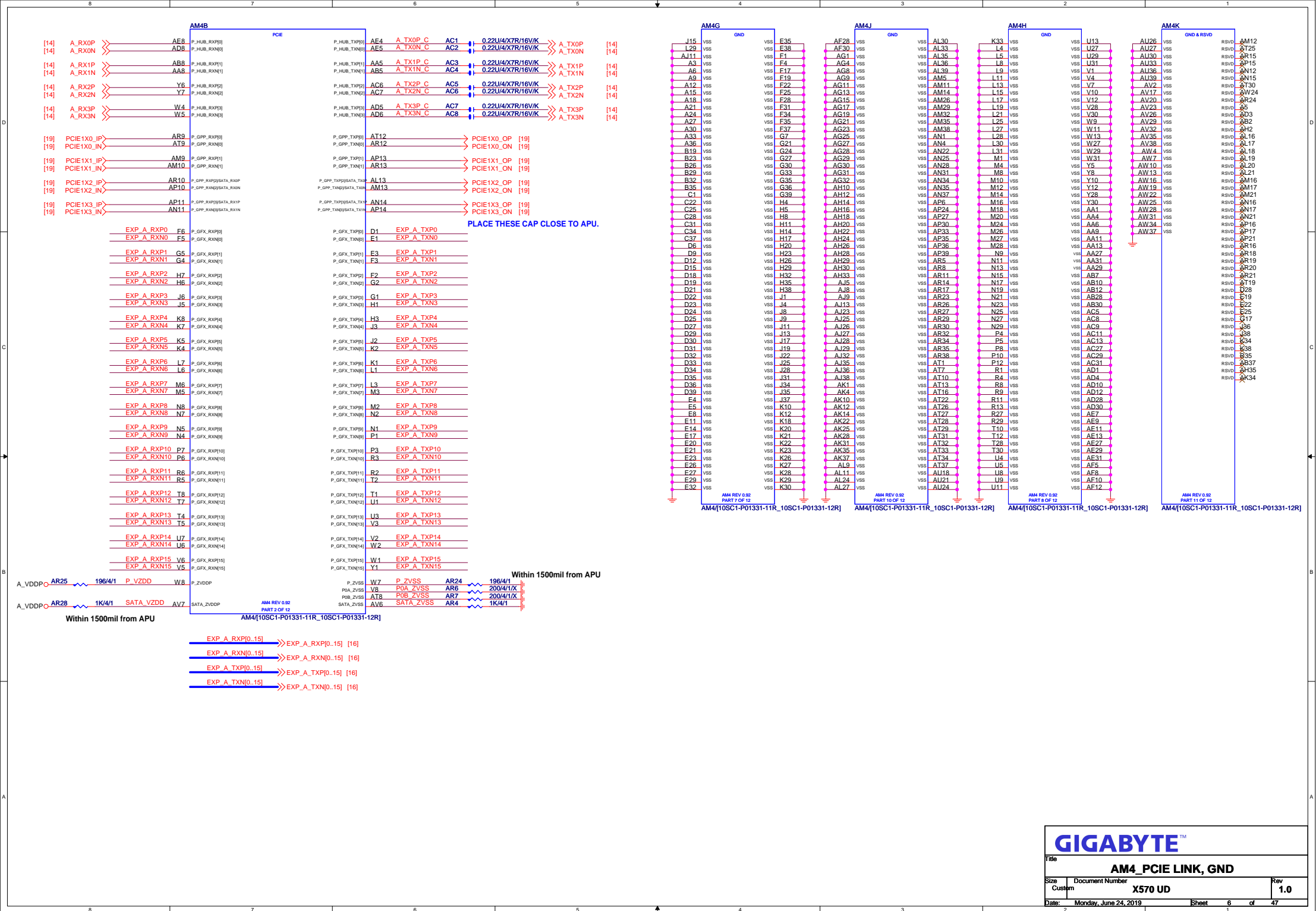
CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h-6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h-0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h-1 Fh	TYPE 3

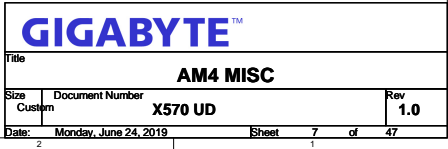
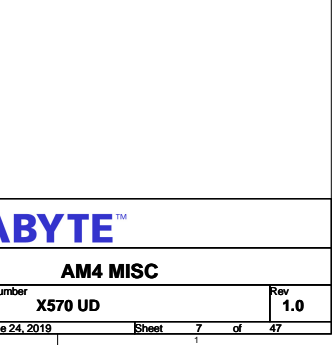
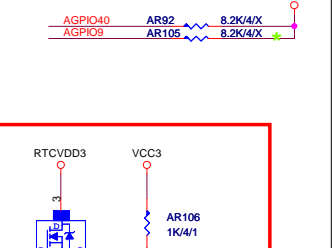
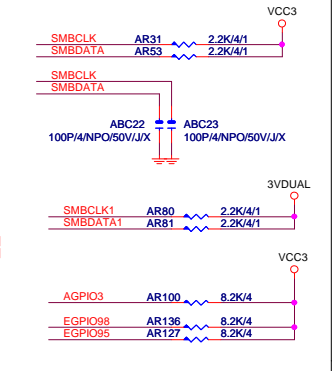
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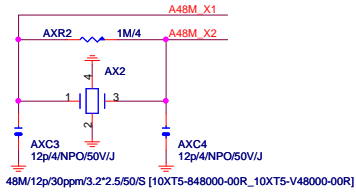
Title: **CPU CONTROL**

Size: Custom Document Number: **X570 UD** Rev: **1.0**

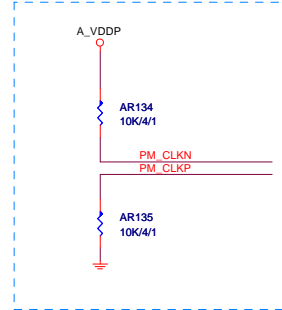
Date: Monday, July 01, 2019 Sheet: 5 of 47



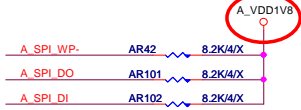




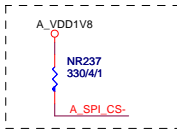
pull up and pull down to the clock from CPU to X570 clock FOR INTERNAL CLOCK GEN project.



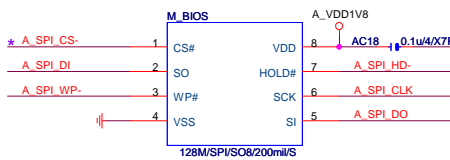
★1.8V SPI ROM USE



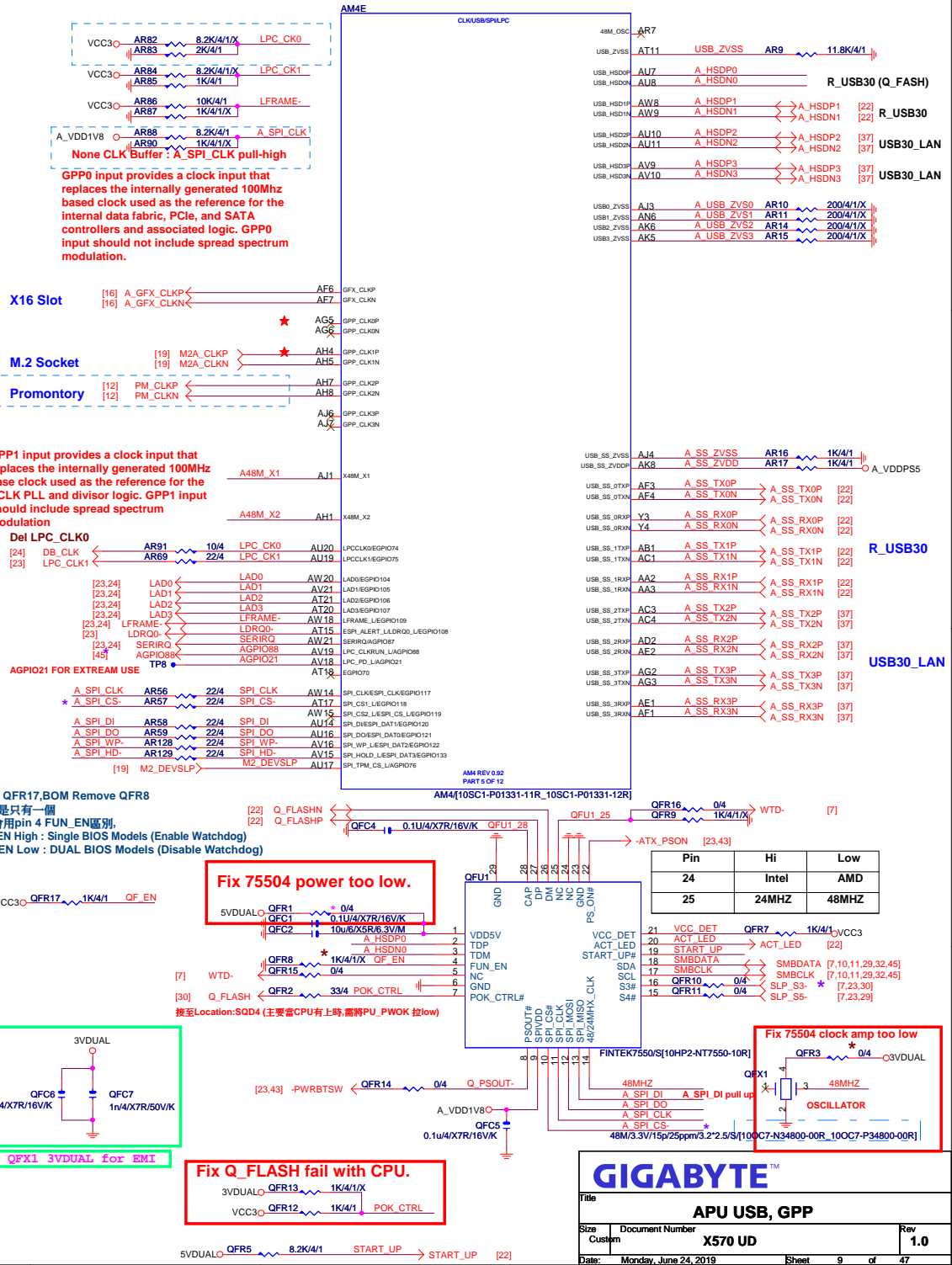
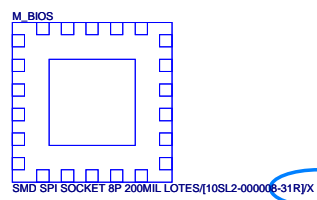
Single (128Mx1) # Layout colay 256Mx1



*PVTI時, M BIOS顆粒, 放在SMD階



FOOTPRINT:IC8WSON-BIOS-COLAY'



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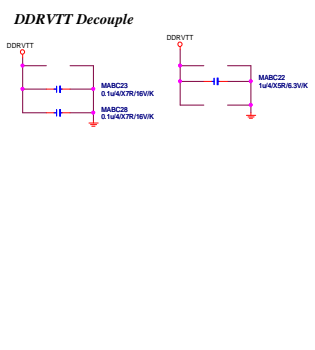
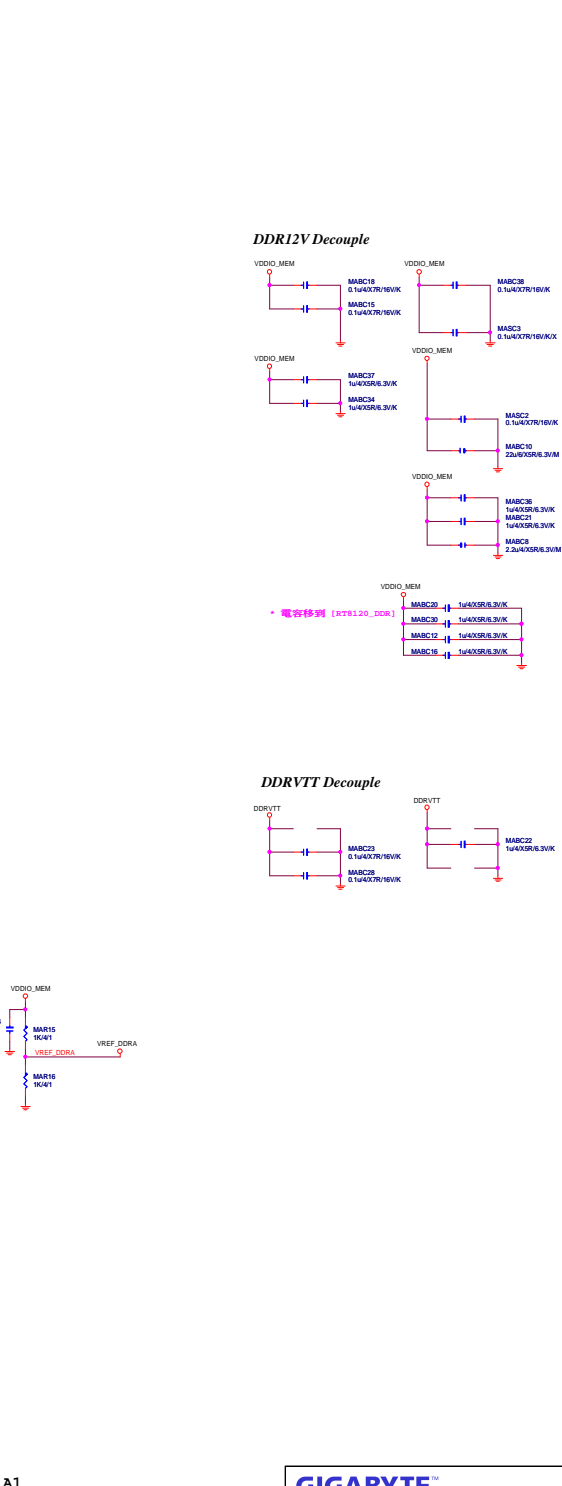
APU USB, GPP

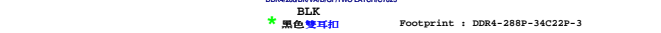
X570 UD

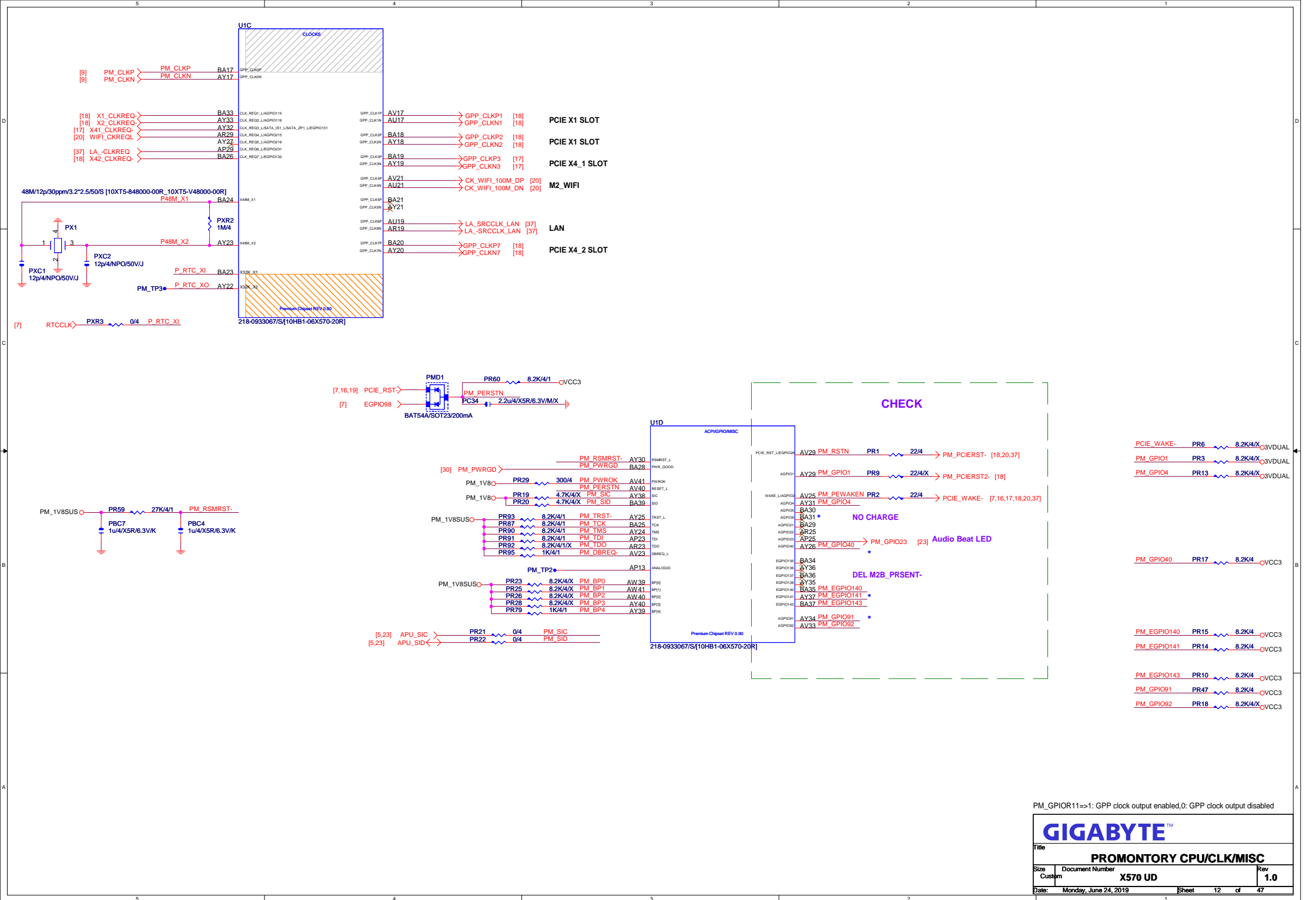
Rev 1.0

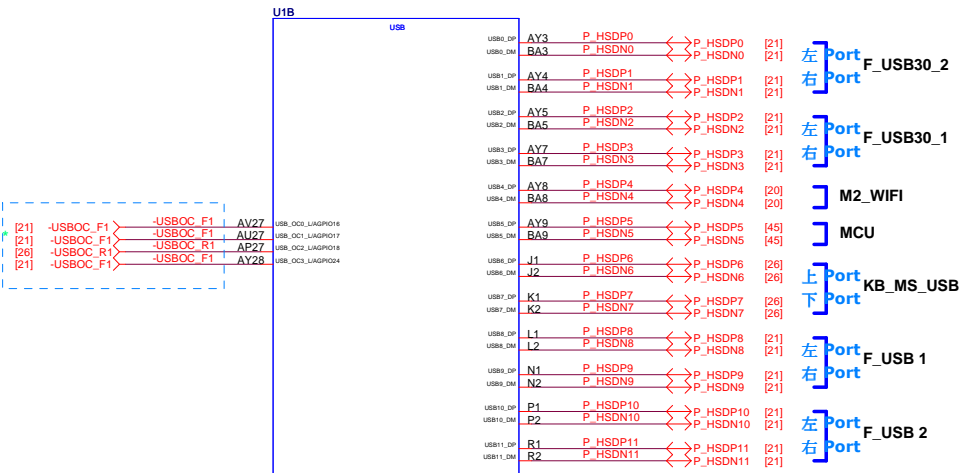
Monday, June 24, 2019

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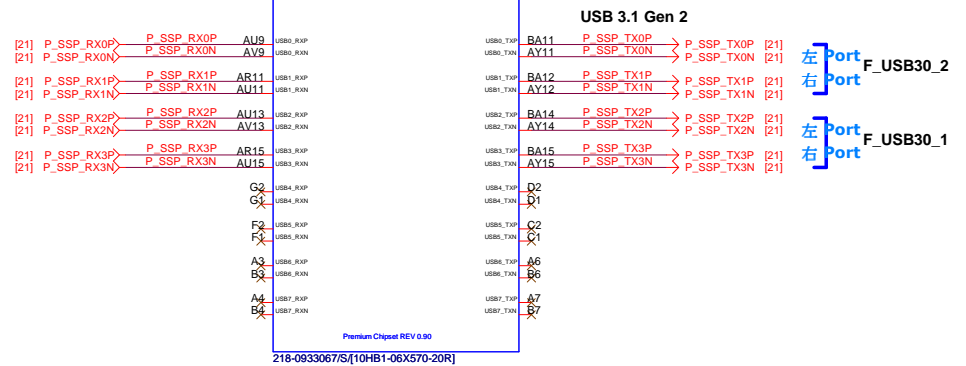




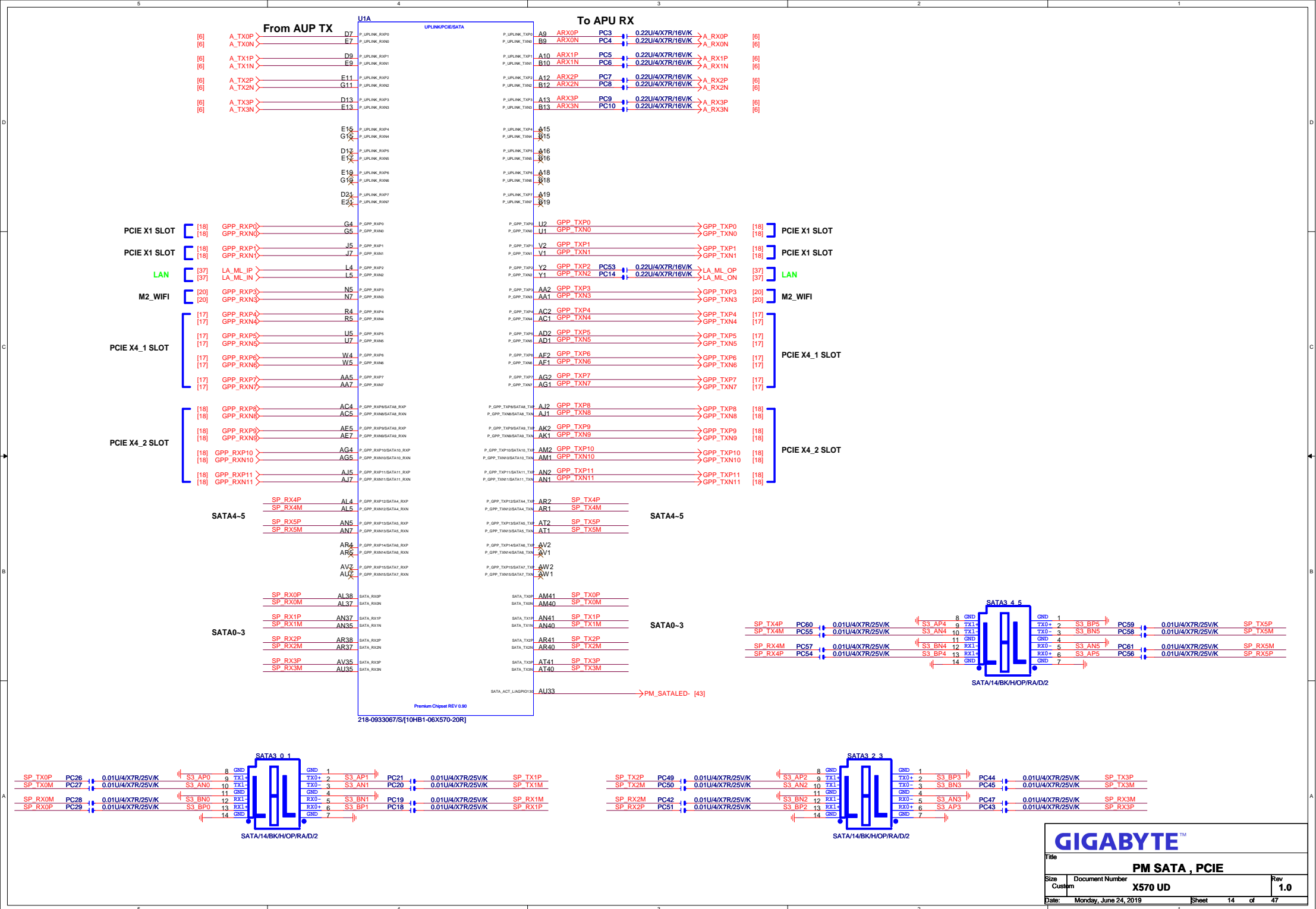


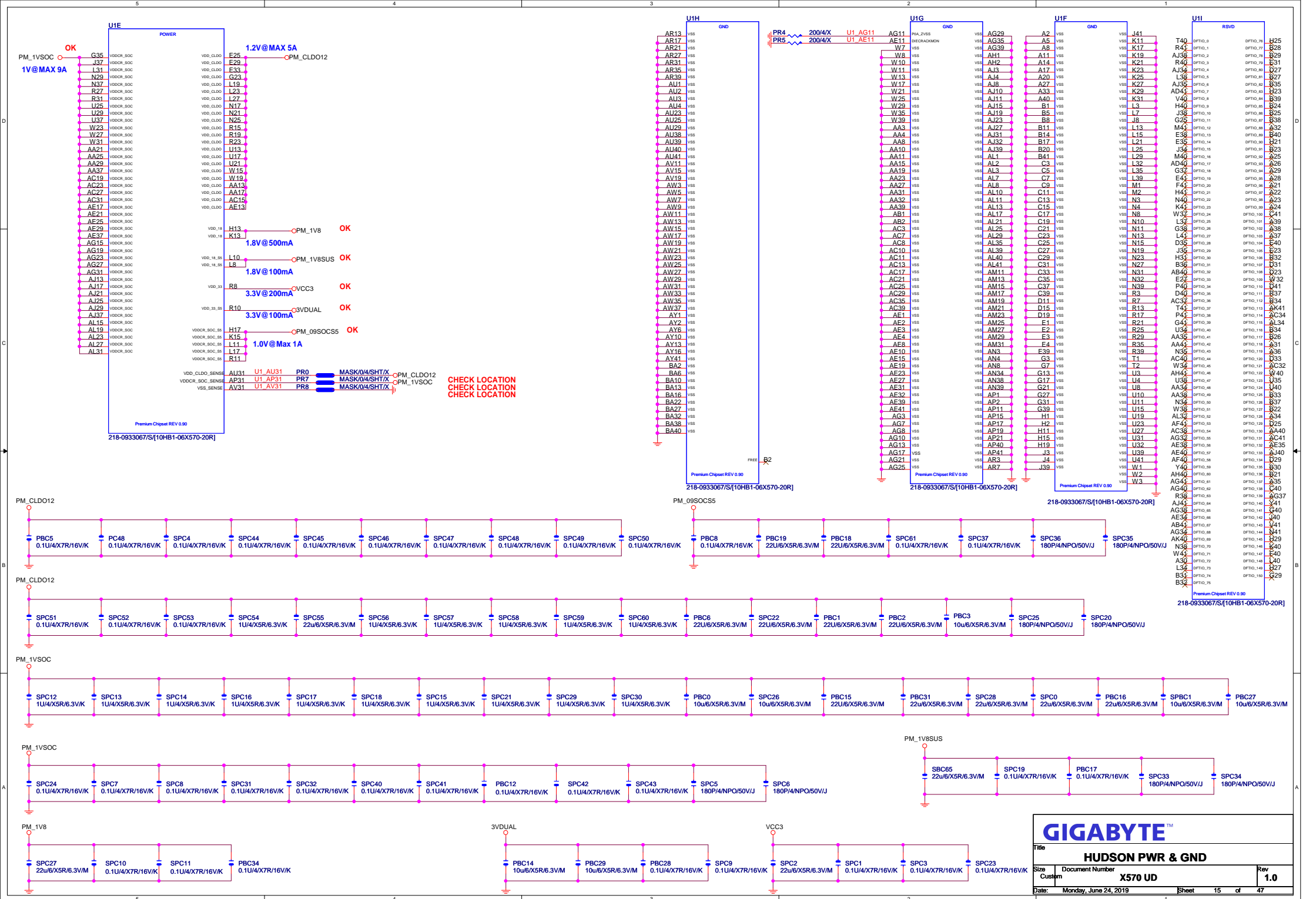


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USB Controller 0: USB20 [0:5], USB30 [0:3]		HSD 10	
USB Controller 1: USB20 [6:11], USB30 [4:7]		HSD 11	
USB30G2		HSD 6	
USB20		HSD 7	
0		HSD 8	
1		HSD 9	
2		HSD 5	
3			
4			
5			
6			
7			





FOR SMBUS
PCIEX16不能short pad,不上件

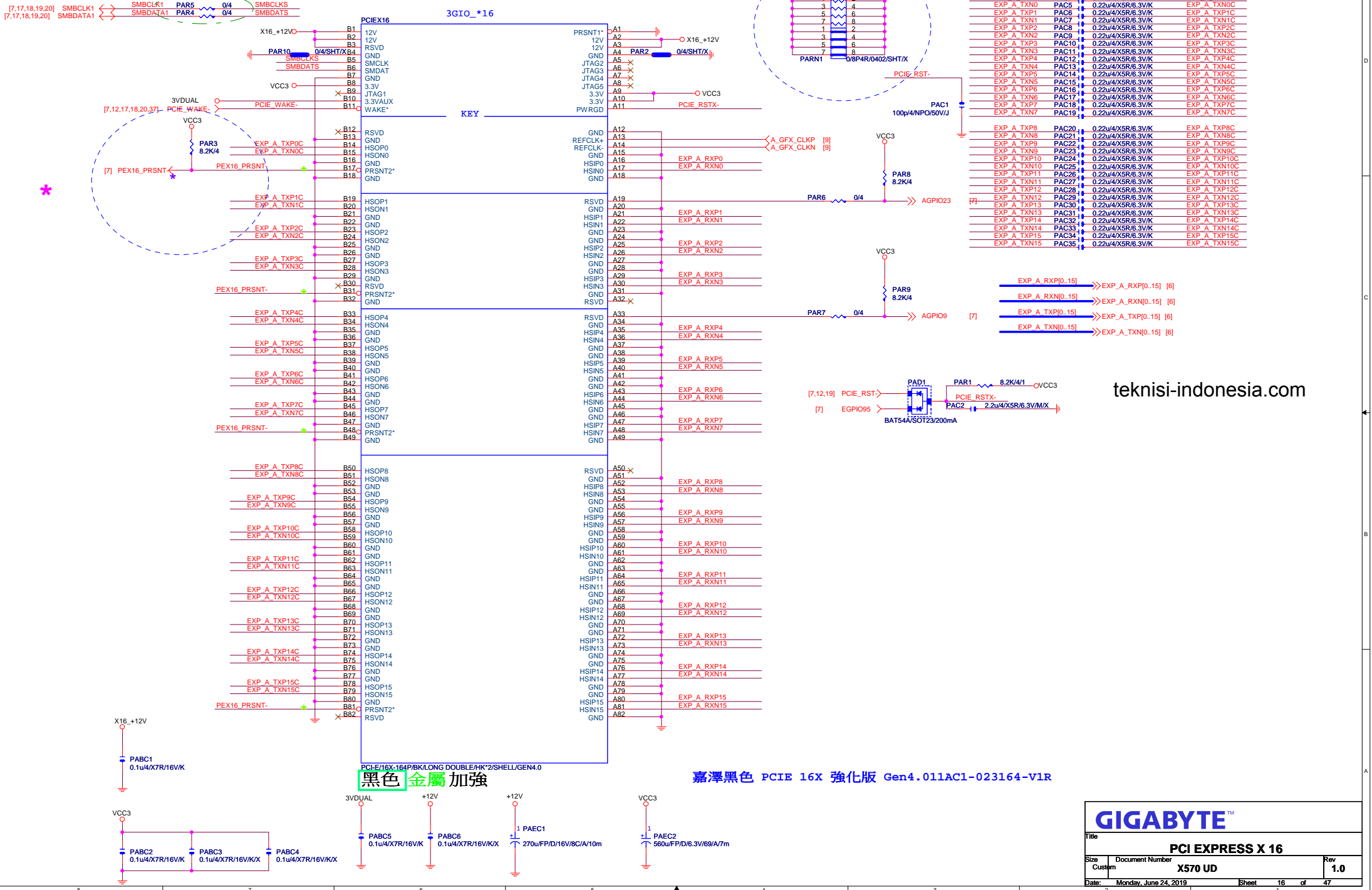
[7,17,18,19,20] SMBCLK1 <-- SMBCLK1 PAR5 0/4 SMBCLKS
[7,17,18,19,20] SMBDATA1 <-- SMBDATA1 PAR4 0/4 SMBDATS

Footprint :
PCIESLOT-1648TH

3GIO_*16

+12V - protect
short-wire test

0.22u/4/X5R/6.3V/K, Footprint:C0402-2



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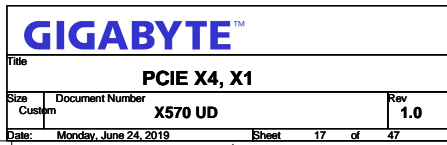
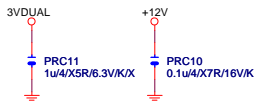
GIGABYTE™		
Title PCI EXPRESS X 16		
Size Custom	Document Number X570 UD	Rev 1.0
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PCIEX4 SM Bus

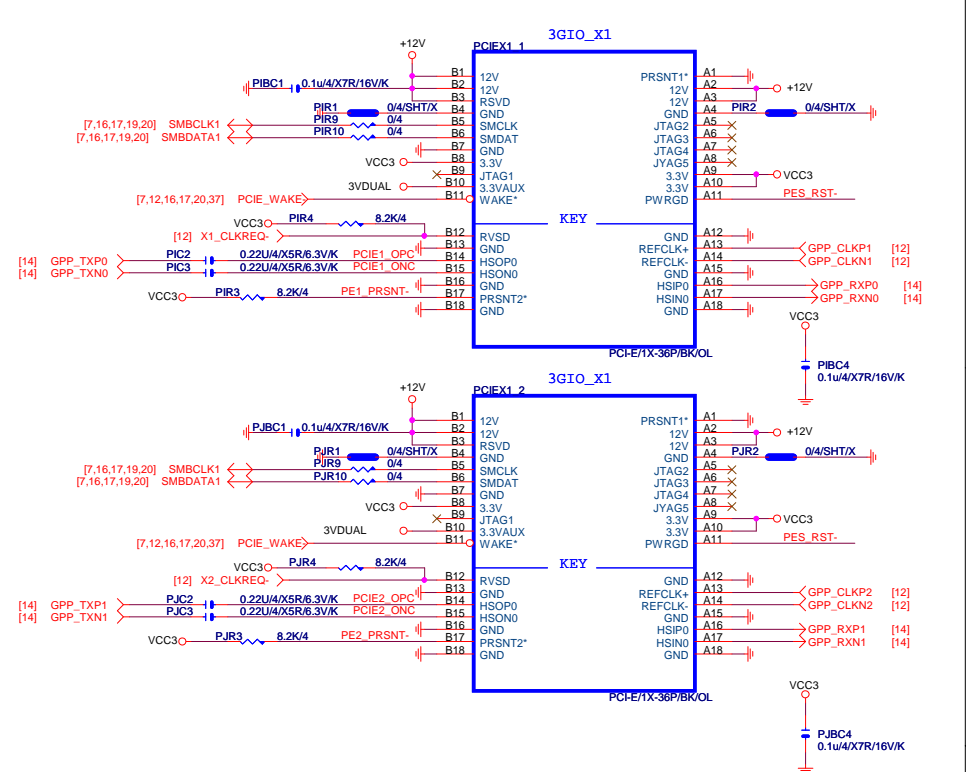
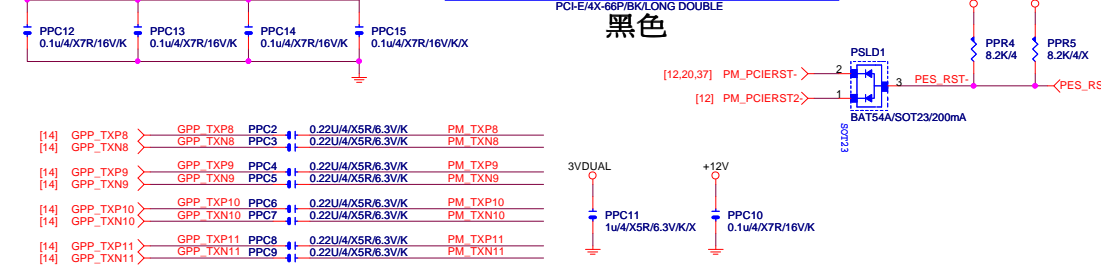
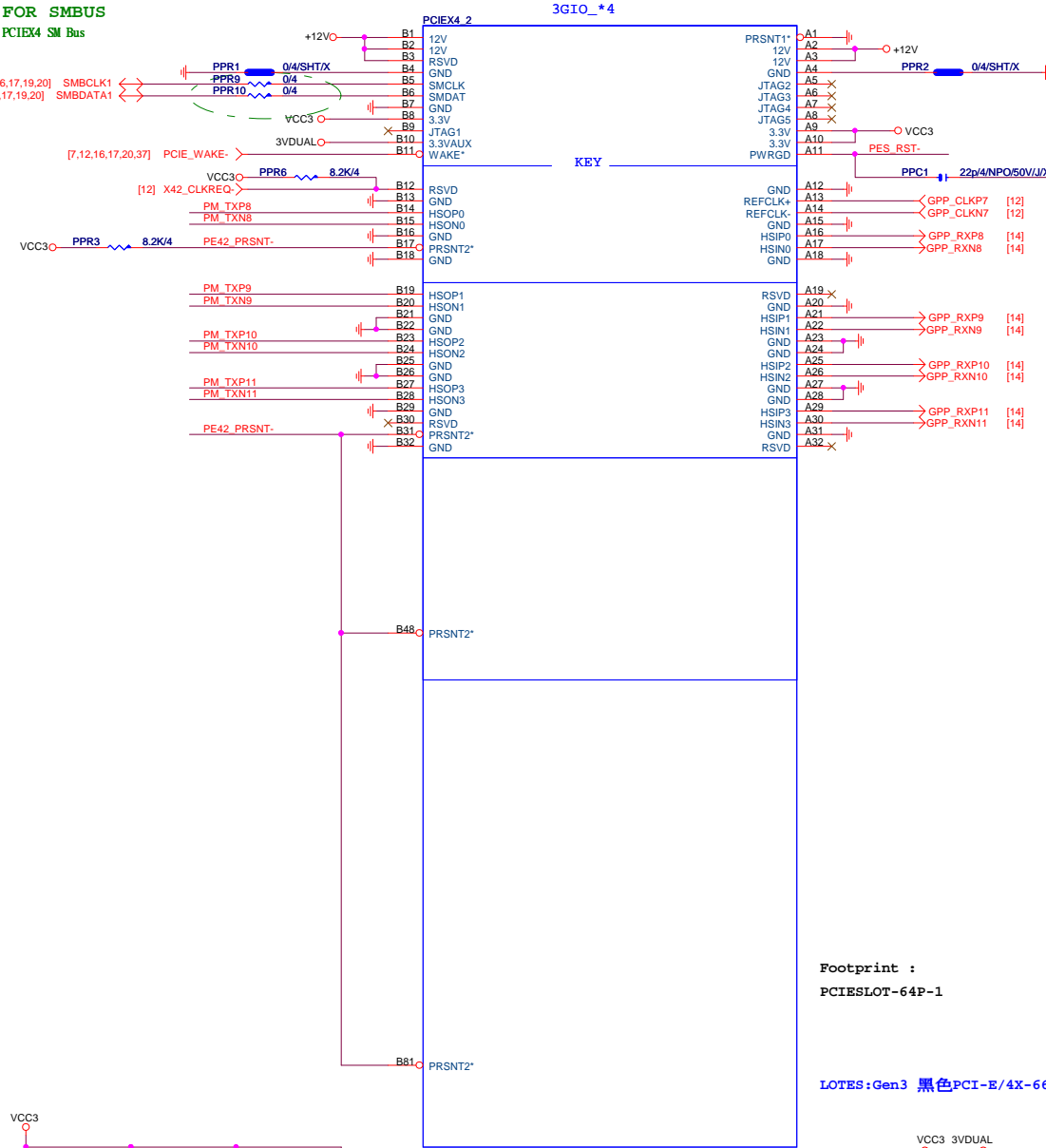
```
16,18,19,20] SMBCLK1
6,18,19,20] SMBDATA1
```



LOTES:Gen3 黑色PCI-E/4X-66P/BK/LONG DOUBLE :11AC1-023065-17R



FOR SMBUS
PCIEX4 SM Bus



Footprint :
PCIESLOT-64P-1

LOTES:Gen3 黑色PCI-E/4X-66P/BK/LONG DOUBLE :11AC1-023065-17R

Rev 0.5

REVERSE

CPU P0

CPU P1

CPU P2

CPU P3

SATA : GND. PCIE : NC

M2A_SOCKET

SKT3
SSD PIN OUT

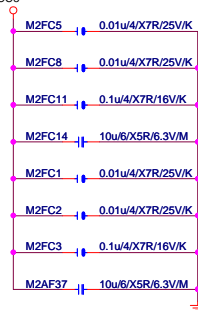
KEY M

M267/BK/RA/S/H8.5mm/M KEY/SHELL/DIP+4HS T1.0/GEN4.0[10NR5-130M67-61R]

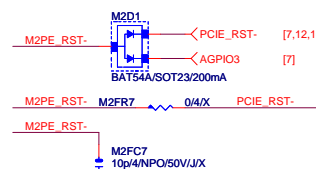
架高 無鐵殼

Footprint : M2_110

VCC3



AMD CPU PCIE FIX



DIP螺柱



加高

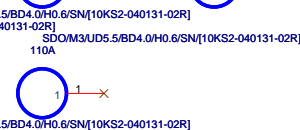
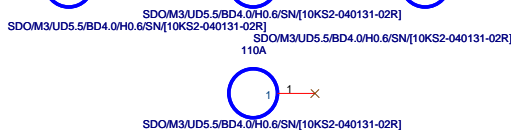
110A



CR[12KS2-110202-01R]

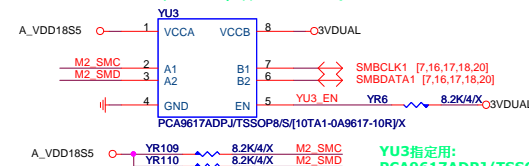
DIP螺絲

SMD螺柱



刪除SMD螺柱文字面 "A" ,不要show 出在PCB文字面上

M.2 Level Shift for M.2 & PCIE slot的SMbus,可控RGB M.2/AIC SSD.



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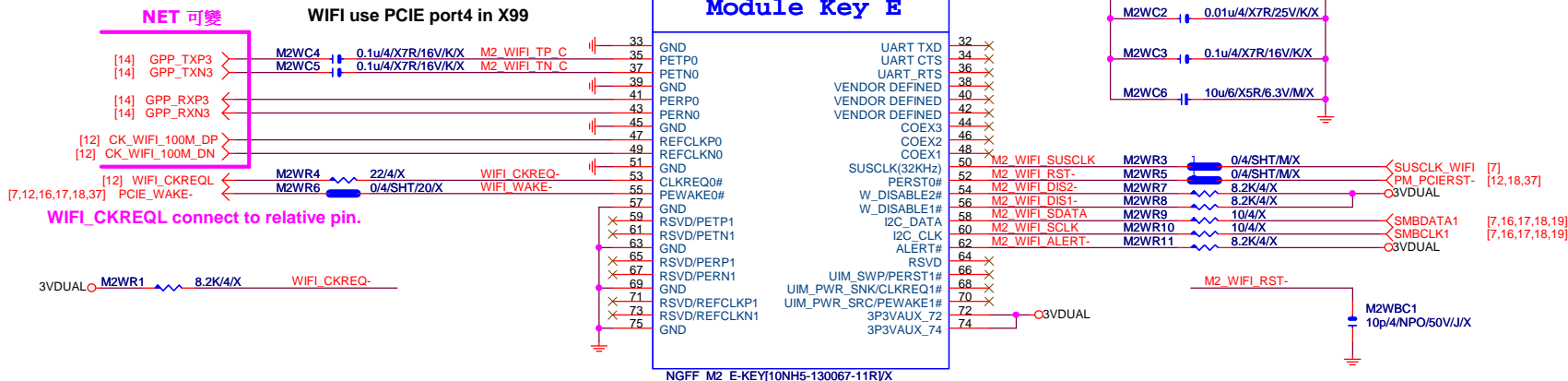
Title			
M.2 SLOT FROM CPU(A)			
Size	Document Number	Rev	
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Date:	Wednesday, July 03, 2019	Sheet	19 of 47

Rev: 0.2 *全部不上件

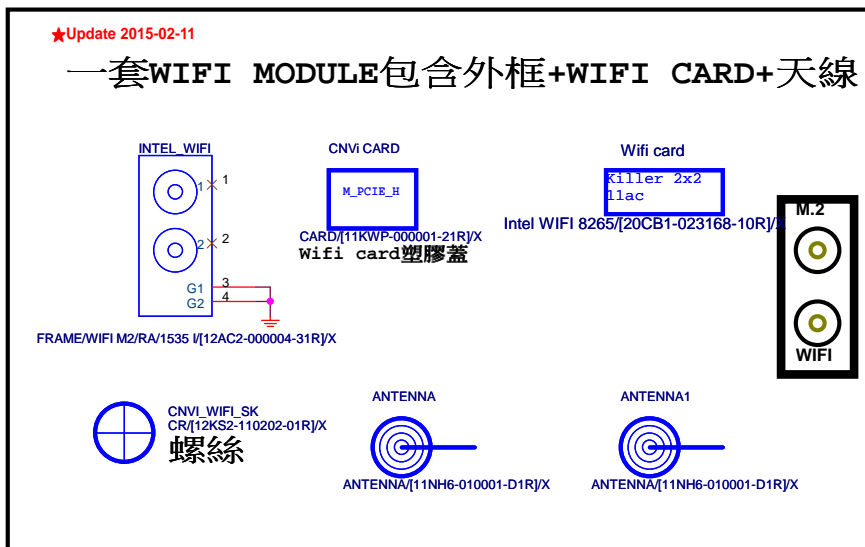
請選擇適用的USBport :
SOC/UD7/UD5/G1/G7 : USB4
iUD3/G5:USB6

PCIE:15/4/4/15(breakout min 8/4/4/8)
外層Impedance=85 +- 17.5%

PCIE:15/4/4/15(breakout min 8/4/4/8)
內層 Impedance=85 +- 12%



FOR M.2 WIFI MODULE @ REAR PANEL



PCIE:15/4/4/15(breakout min 8/4/4/8)
內層 Impedance=85 +- 12%

直立 Footprint Notice.

★Update 2015-07-22

★Footprint for 直立式 SMD:
WIFI-EKEY
★SMD P/N: 直立式
10NH5-130067-11R.

Rev:0.6
★ for PCIe mode 預留

★ 橫躺式高SMD
P/N:10NR5-130067-61R
★ 橫躺式矮SMD
P/N:10NR5-130067-22R

橫躺 Footprint Notice.

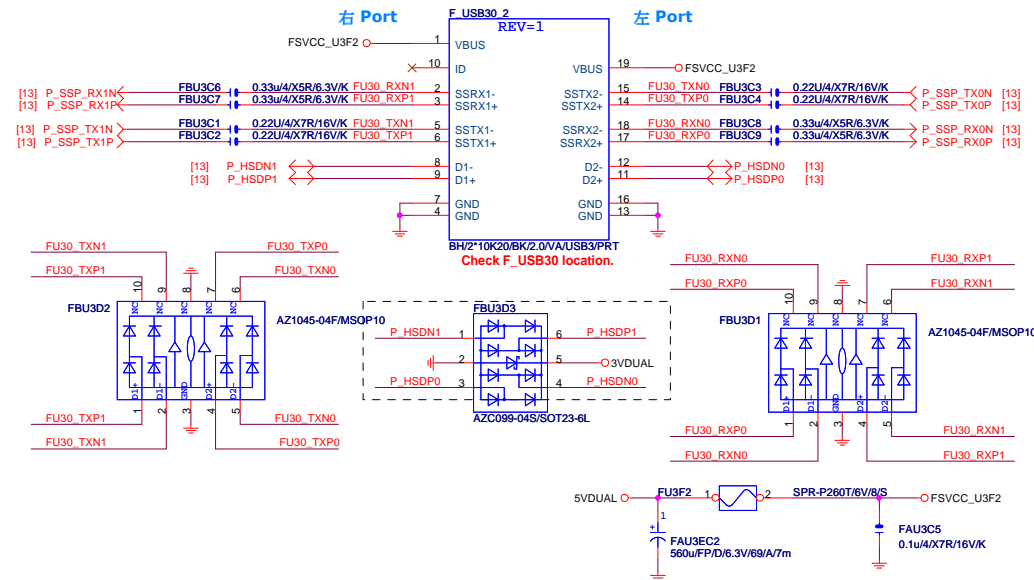
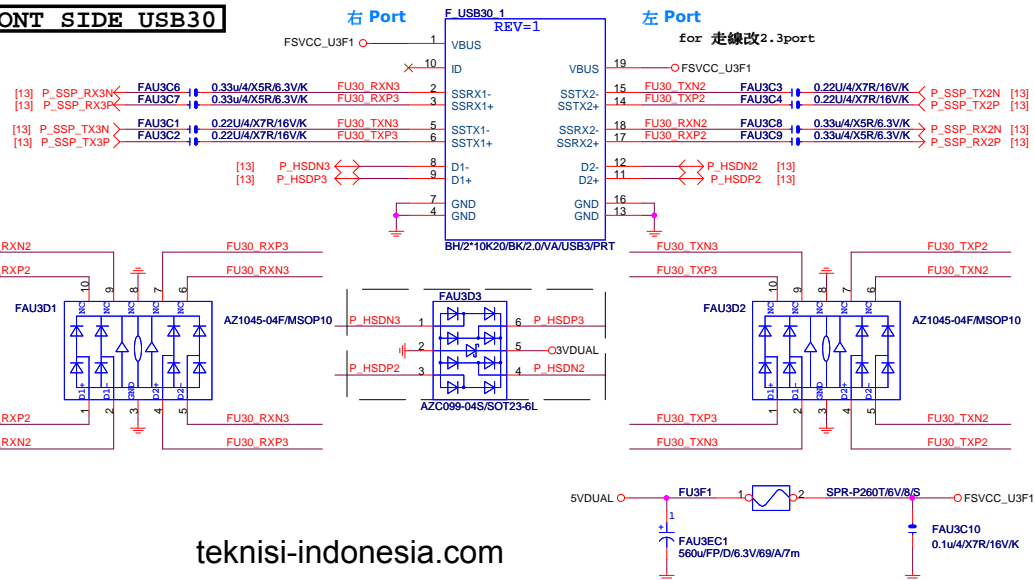
★Update 2015-07-22

★Footprint for 橫躺式高:
NGFF-E-75P-3
★Footprint for 橫躺式矮:
CNV1

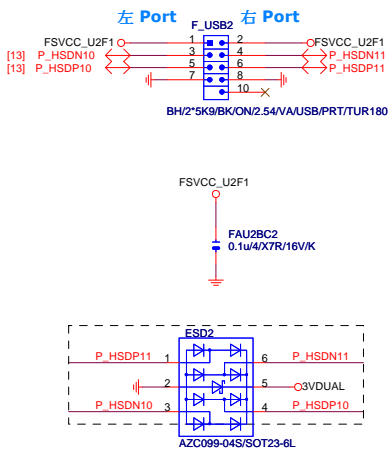
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Title		
M2_WIFI_E_KEY		
Size B	Document Number	Rev
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Date:	Thursday, June 27, 2019	Sheet 20 of 47

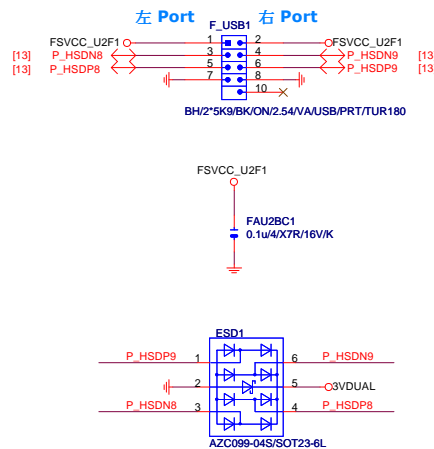
FRONT SIDE USB30



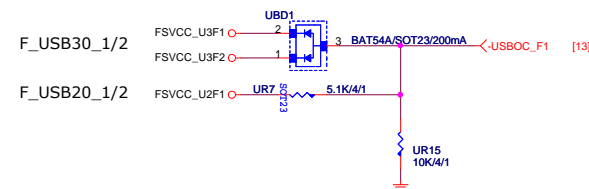
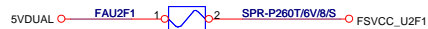
FRONT SIDE USB2



FRONT SIDE USB1

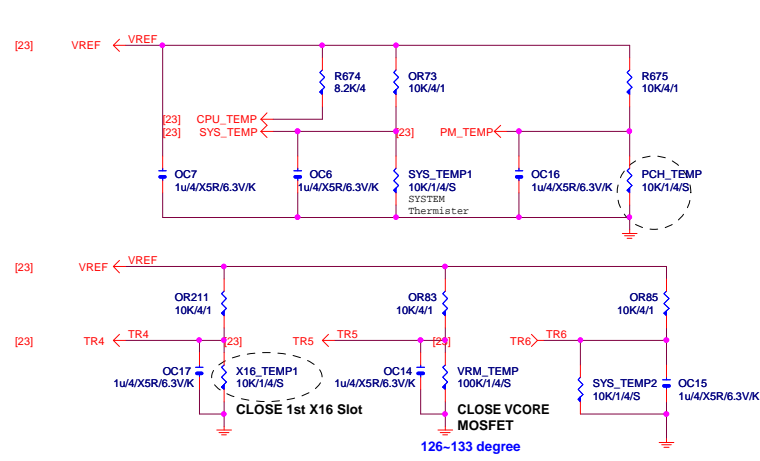


Close to connector
FUSE 2 Port 1 Fuse 2A

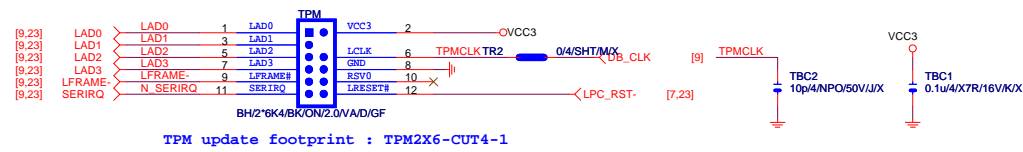
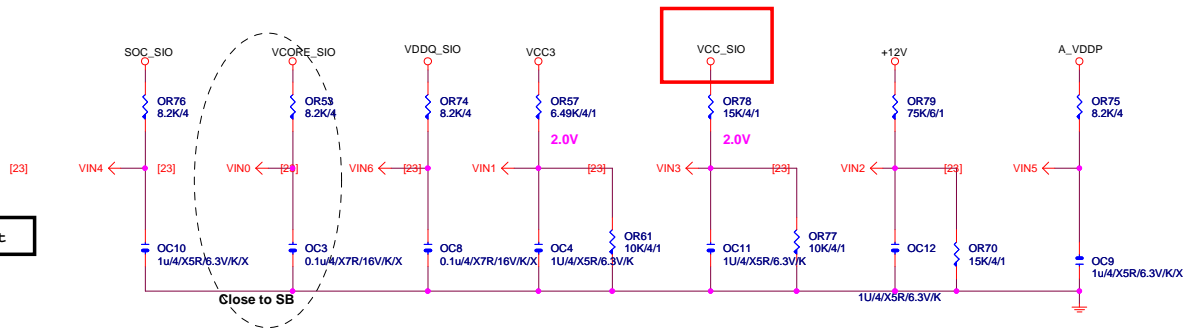


Color markers can be changed by model

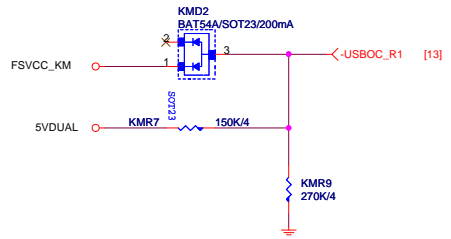
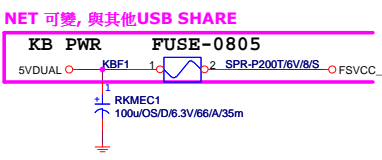
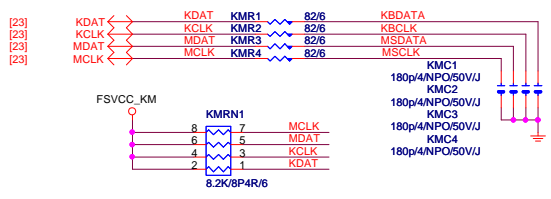
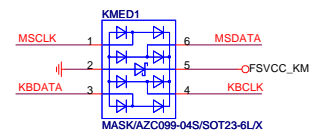
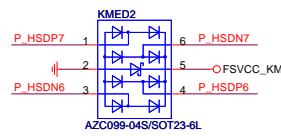
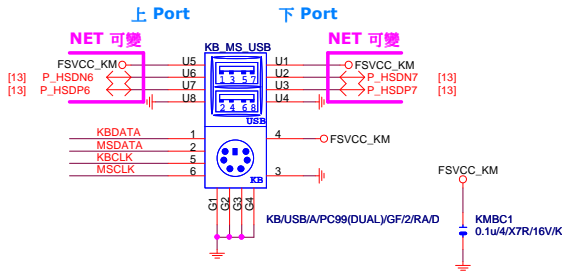
删除clk



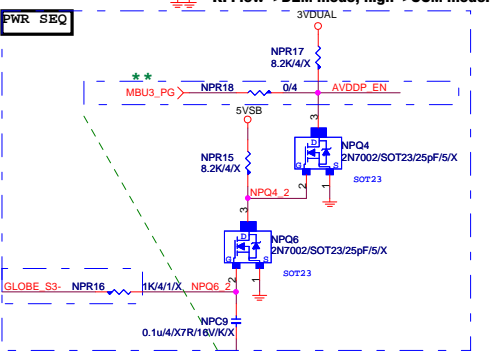
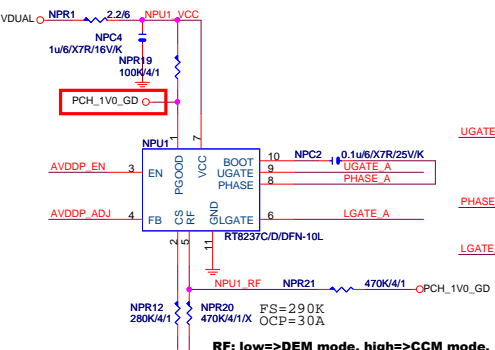
Del Thunderbolt



GIGABYTE™		
Title HWM, TPM		
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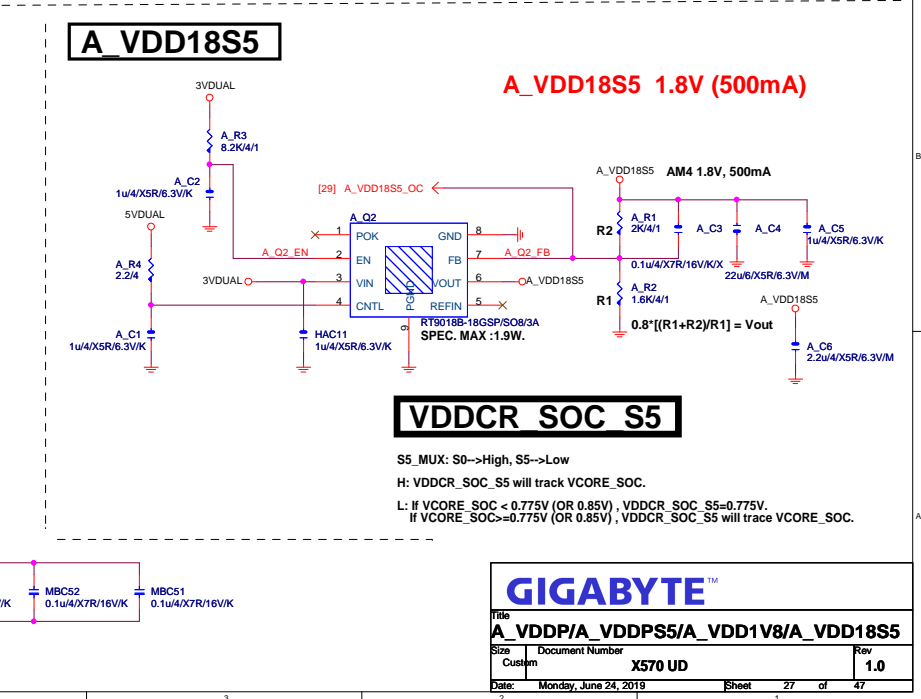
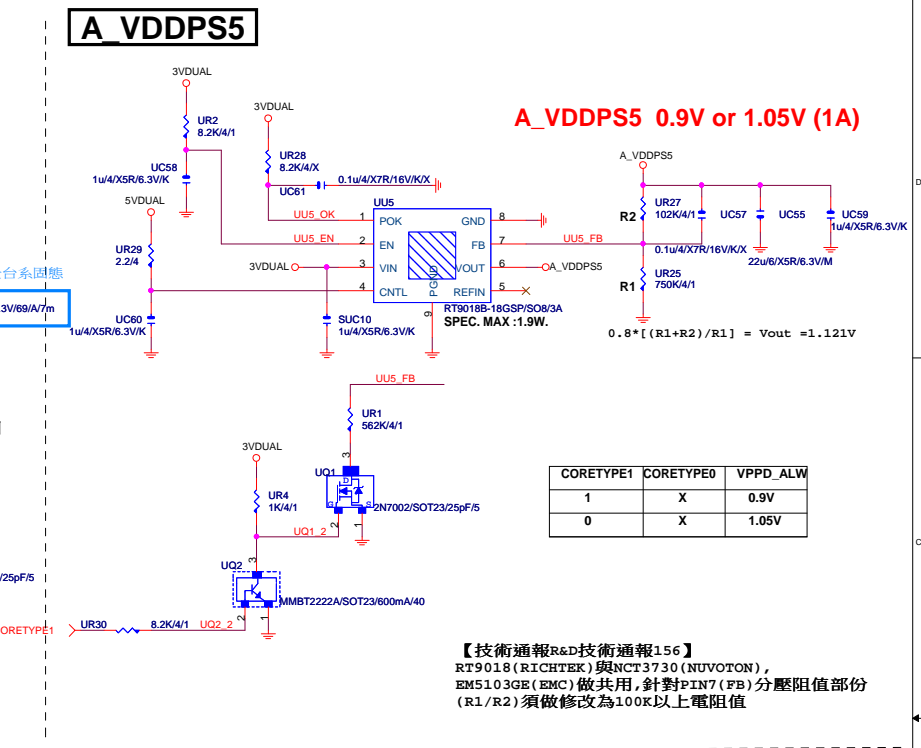
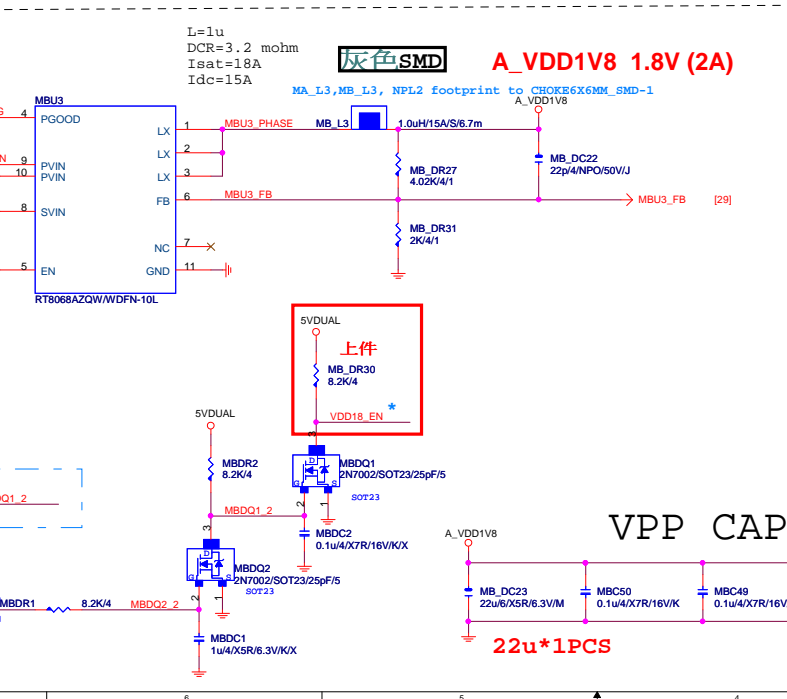
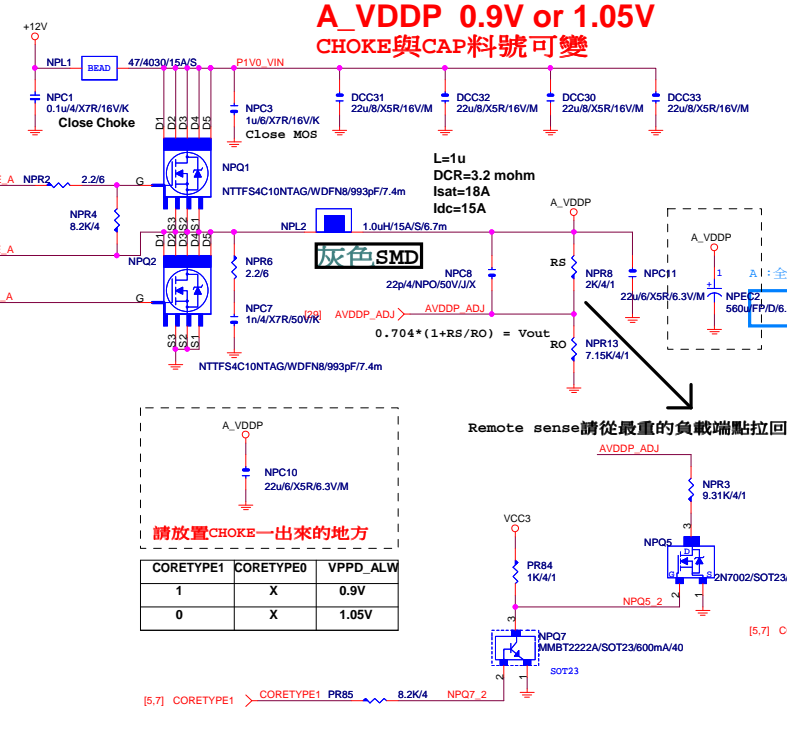
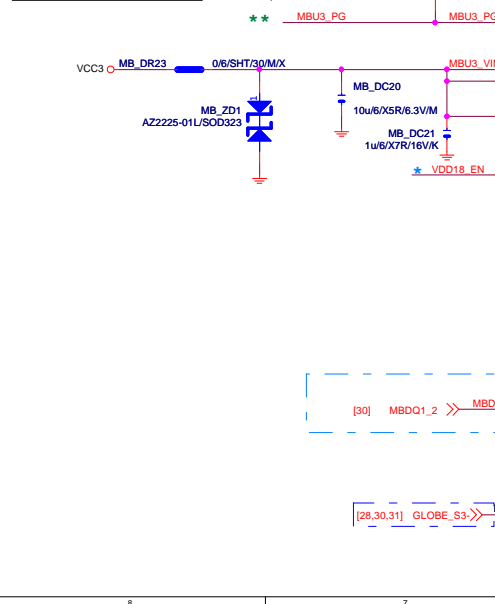


A_VDDP



REV:0.4

A_VDD1V8



VDDCR SOC S5

S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V), VDDCR_SOC_S5=0.775V.
If VCORE_SOC>=0.775V (OR 0.85V), VDDCR_SOC_S5 will trace VCORE_SOC.

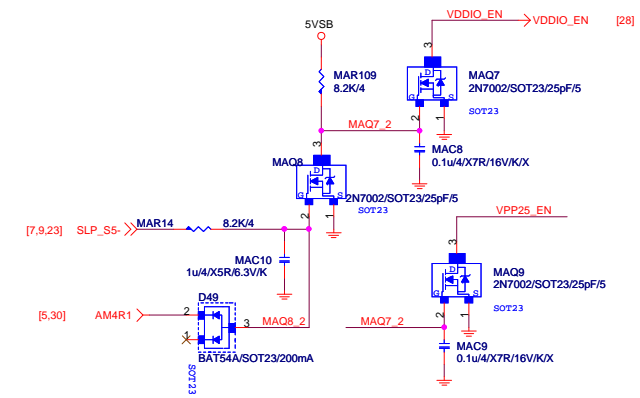
GIGABYTE™

A_VDDP/A_VDDPS5/A_VDD1V8/A_VDD18S5

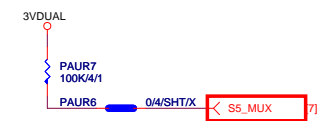
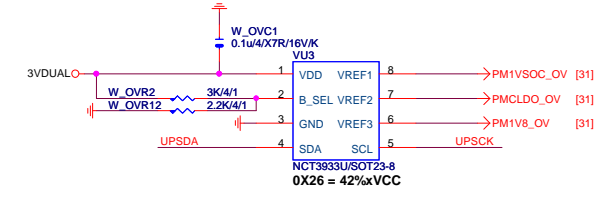
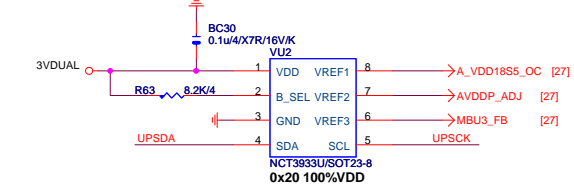
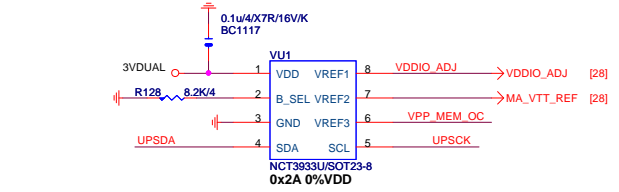
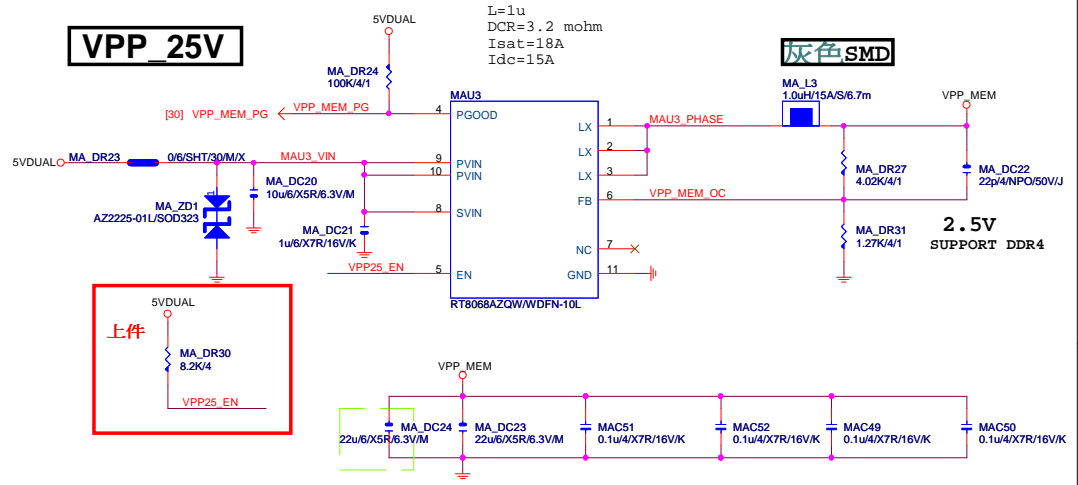
Size: Custom Document Number: **X570 UD** Rev: **1.0**

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PWR_SEQ



VPP_25V

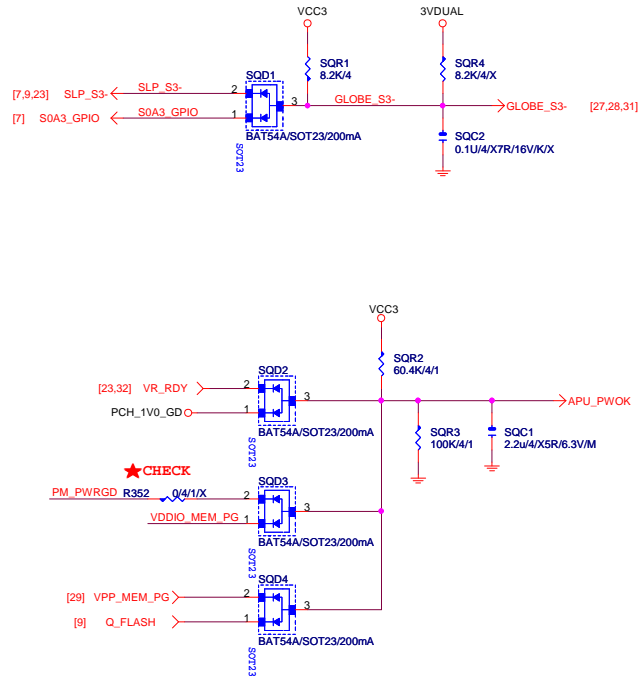


Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

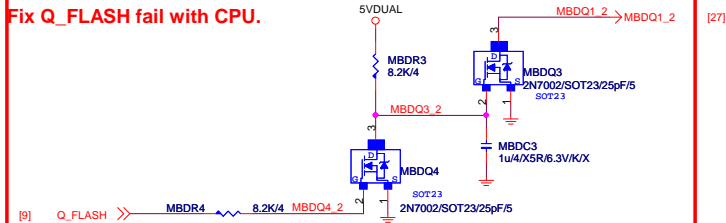
Table1. Recommended Slave Address Setting

GIGABYTE™		
Title		
VPPMEM		
Size	Document Number	Rev
Custom	X570 UD	1.0
Date:	Monday, June 24, 2019	Sheet 29 of 47

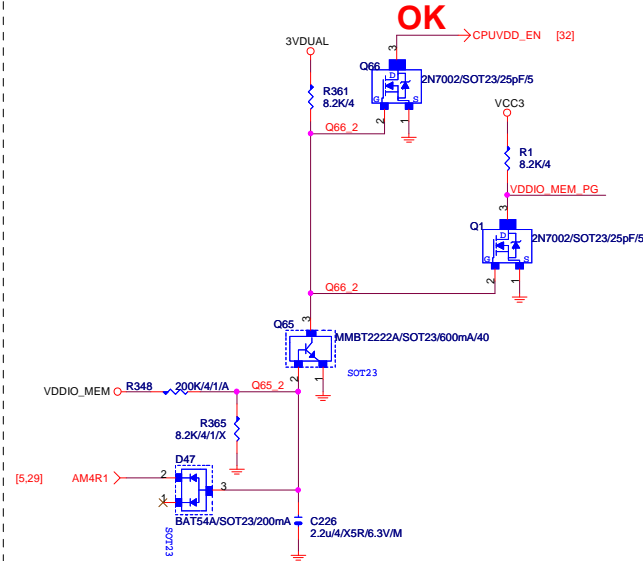
PWR_SEQ



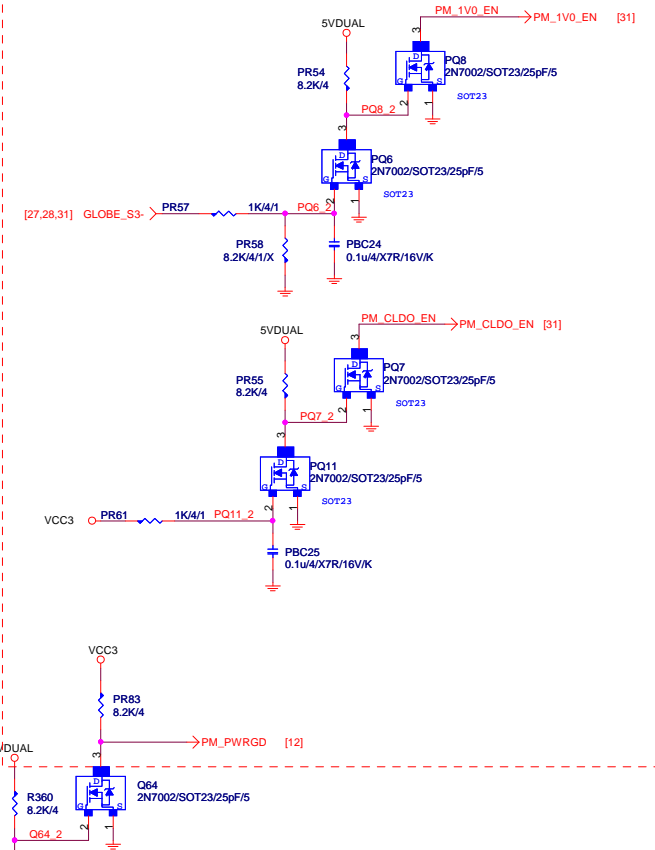
Fix Q_FLASH fail with CPU.



CPU_PWR_SEQ



PM_SWR_SEQ



★ Sequence

APU_PWOK control PM_PWRGD

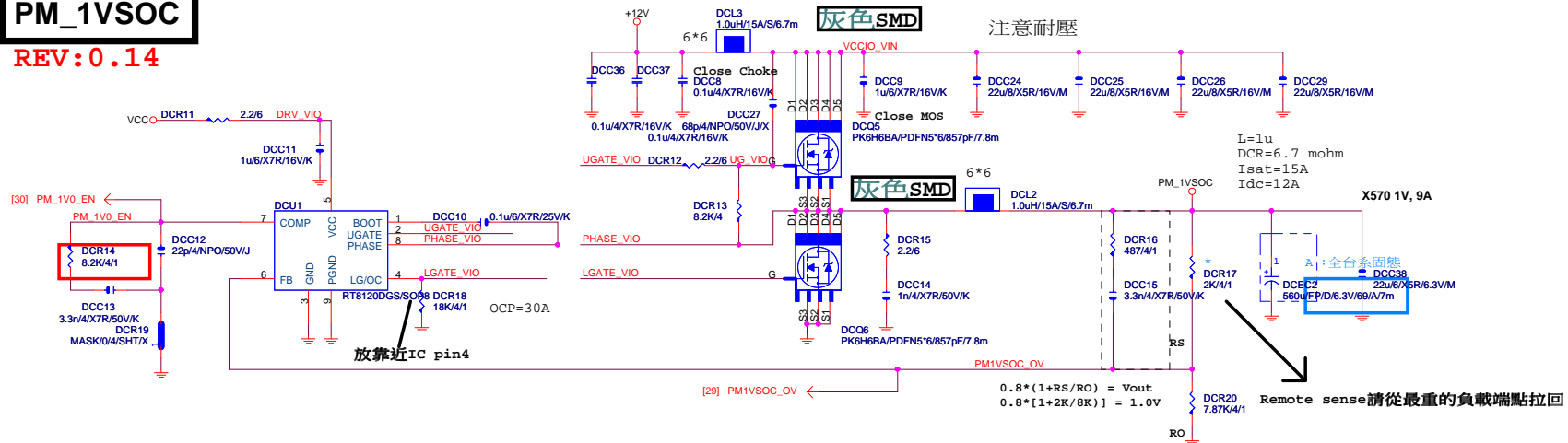


GIGABYTE™

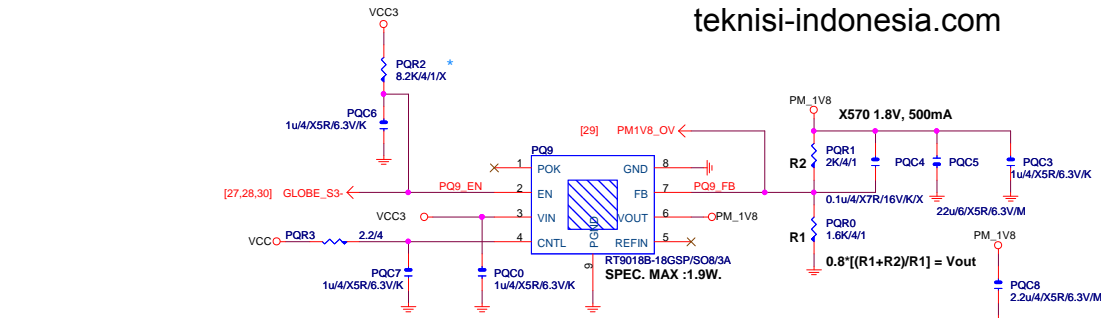
POWER SEQUENCE		
Title	Document Number	Rev
Size	Custom	1.0
Date:	Monday, June 24, 2019	Sheet 30 of 47

PM_1VSOC

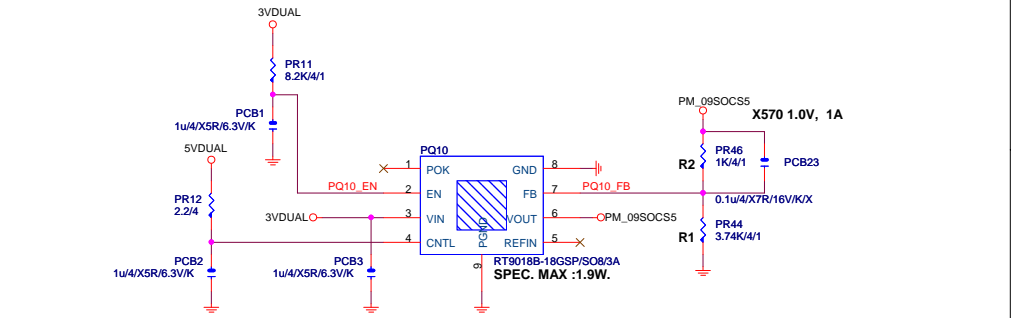
REV:0.14



PM_1V8

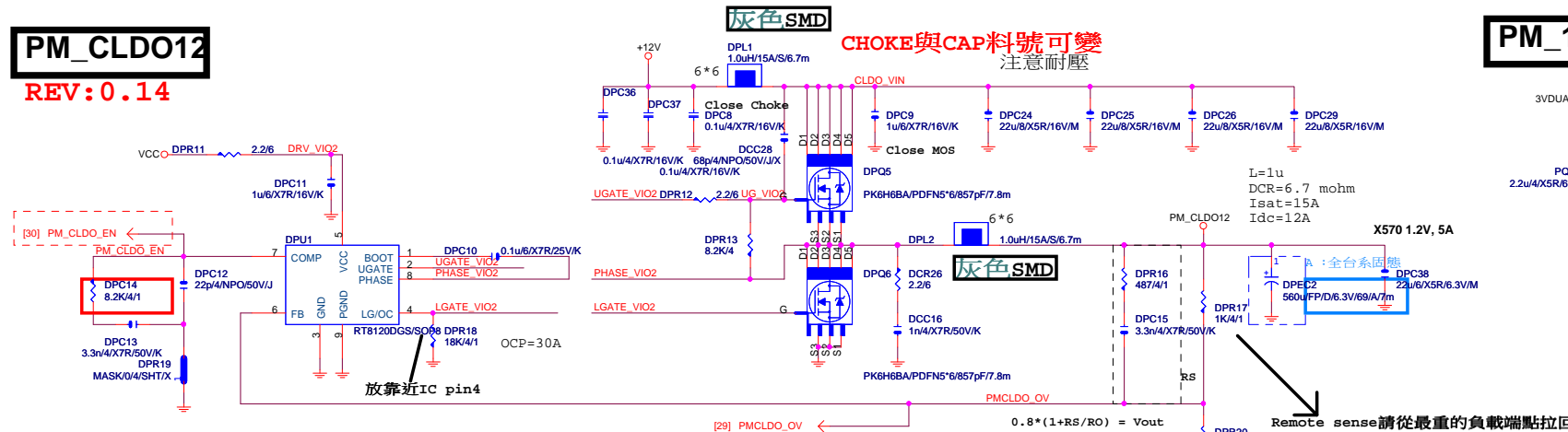


PM_1VSOC_S5

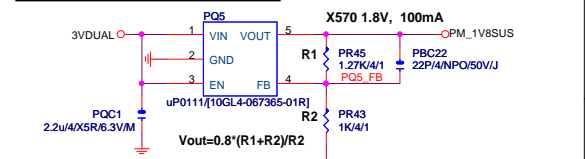


PM_CLDO12

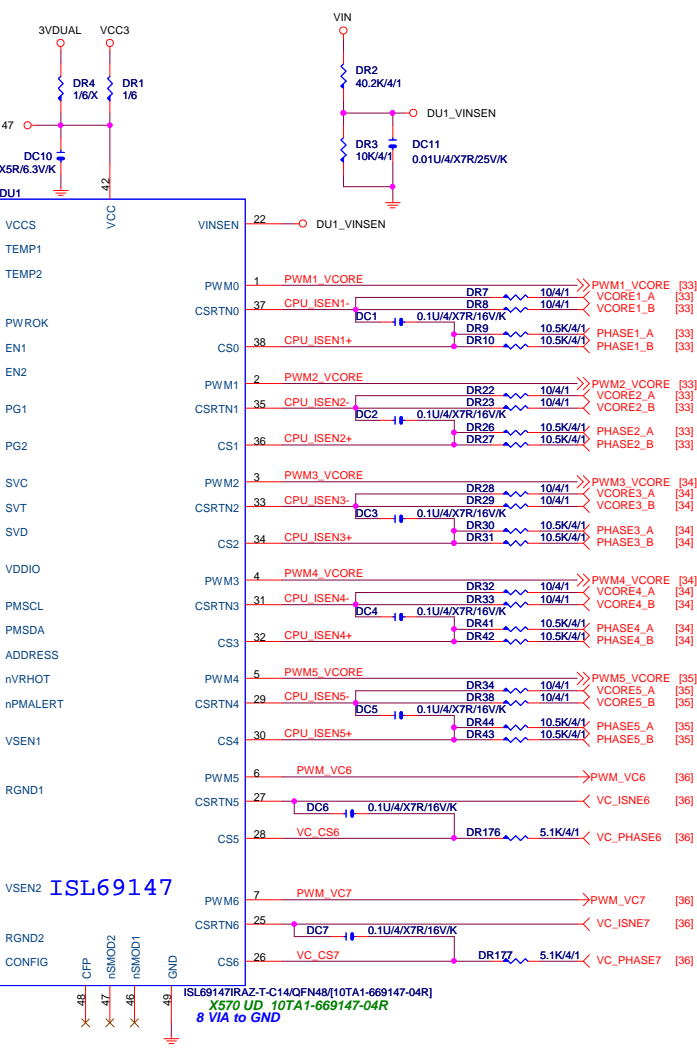
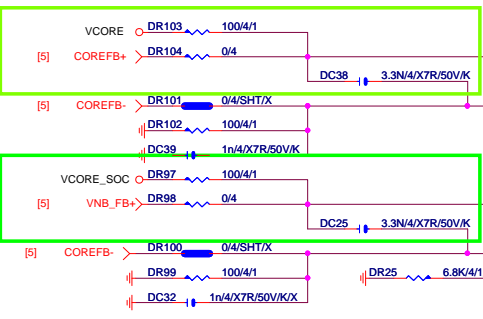
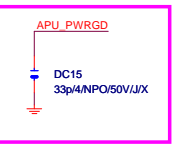
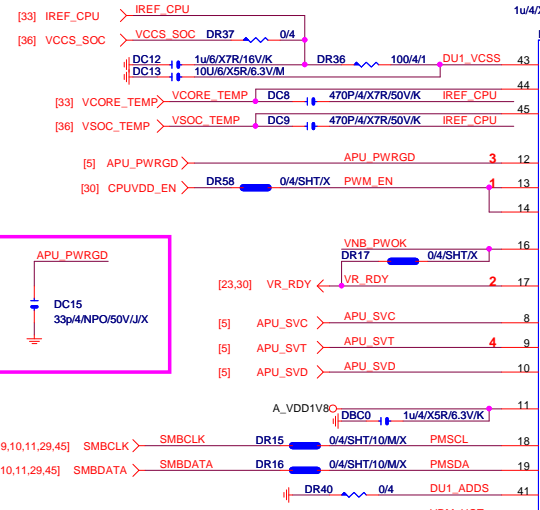
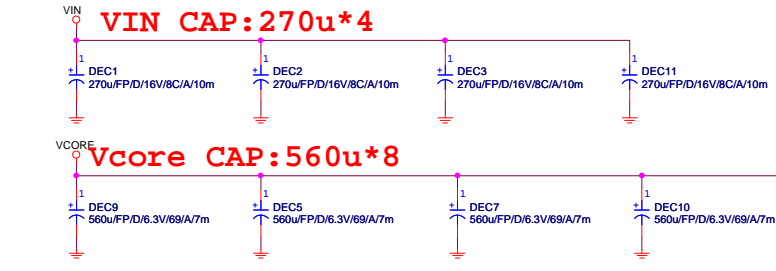
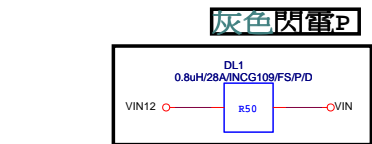
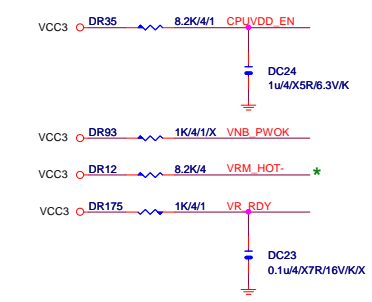
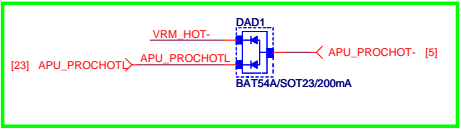
REV:0.14



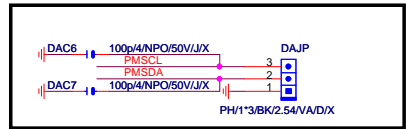
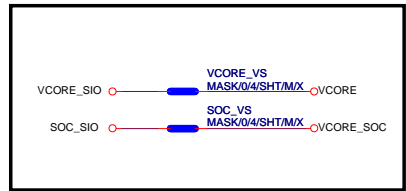
PM_1V8_SUS



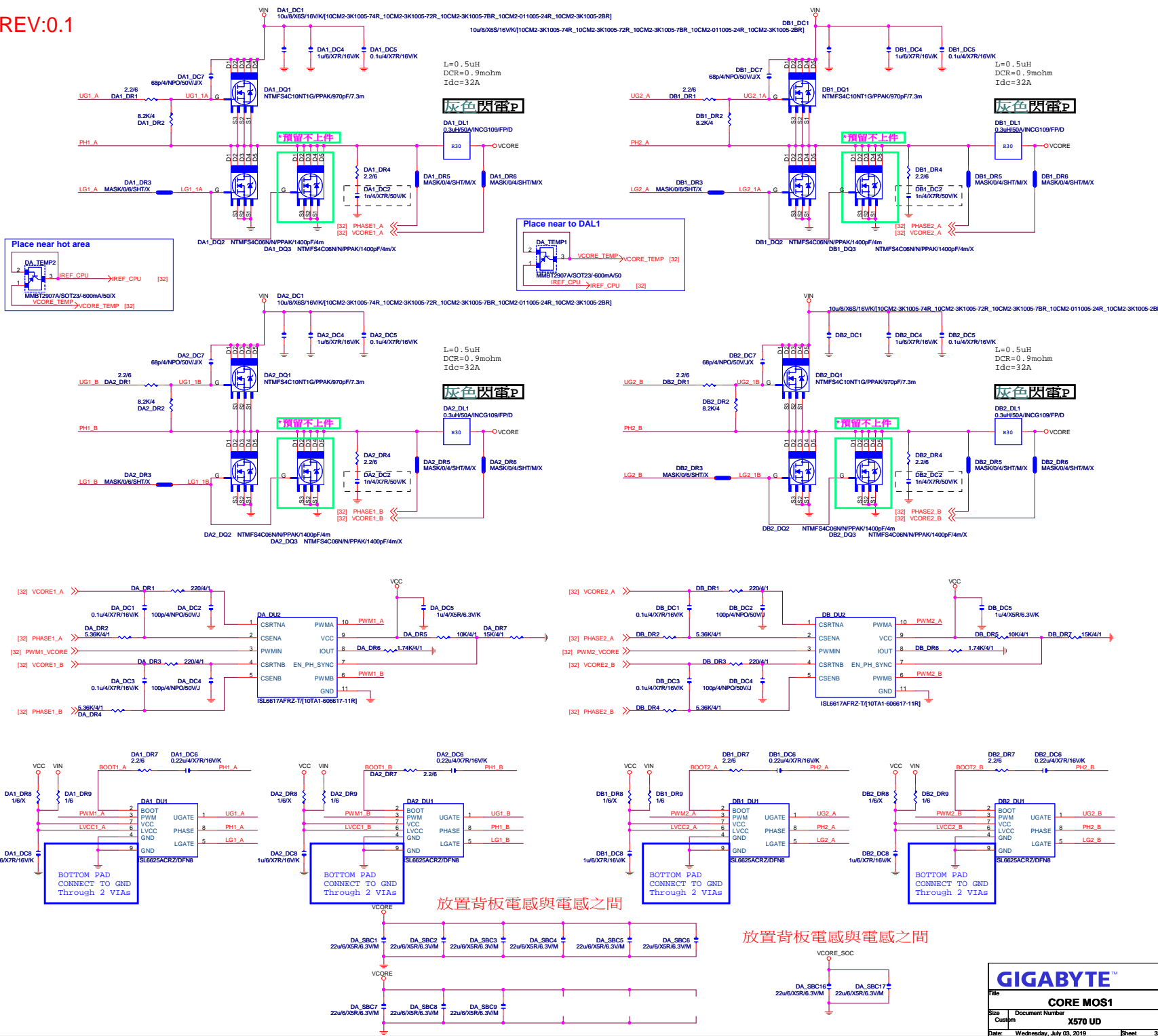
GIGABYTE™			
Title X570 POWER			
Size Custom	Document Number X570 UD	Rev 1.0	
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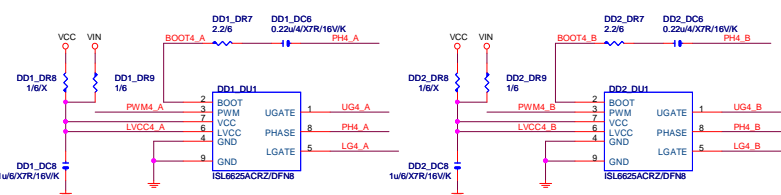
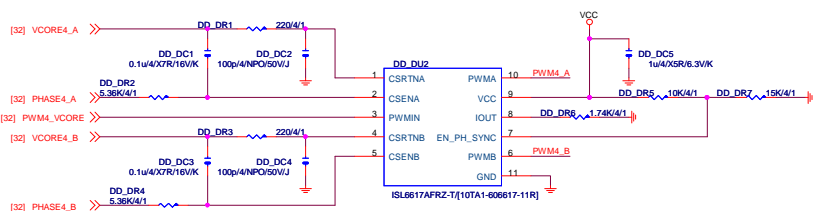
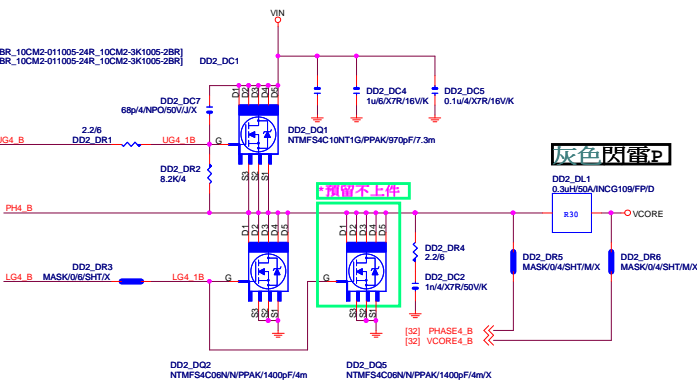
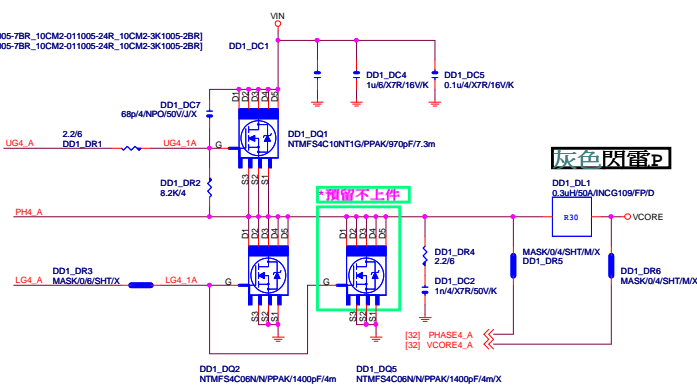


Vcore_SOC CAP:560u*4
LAYOUT 位置空間足夠: NBEC3,NBEC4:SPCAP:330u*2 改成CAP:560u*2

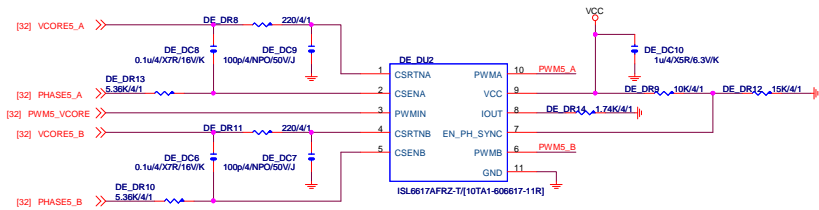
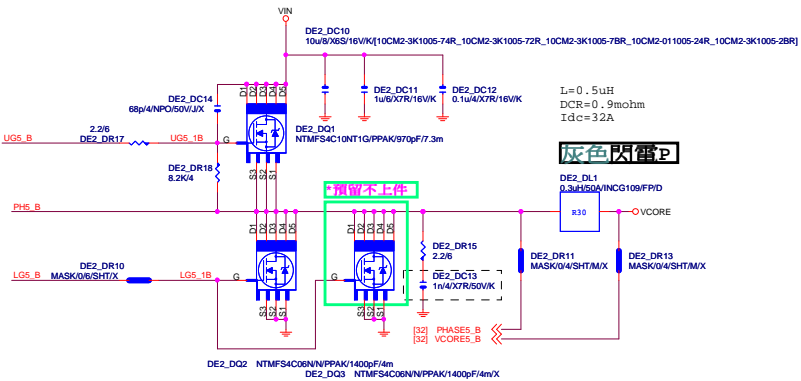
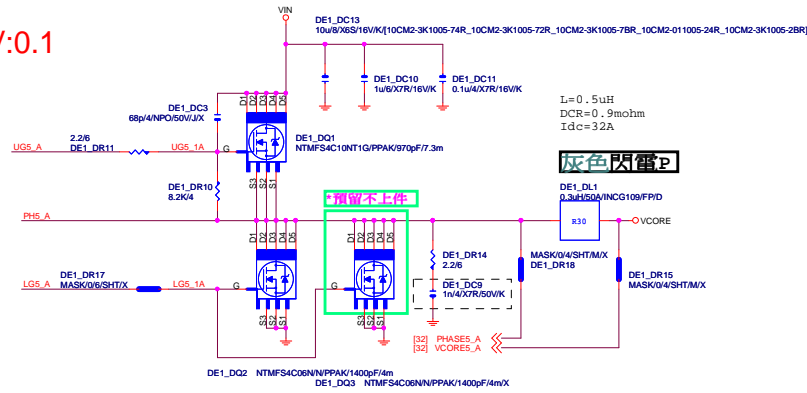


REV:0.1

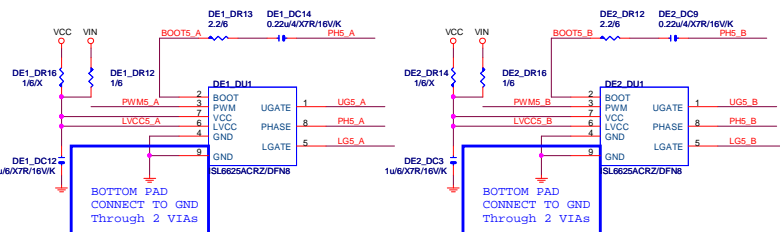


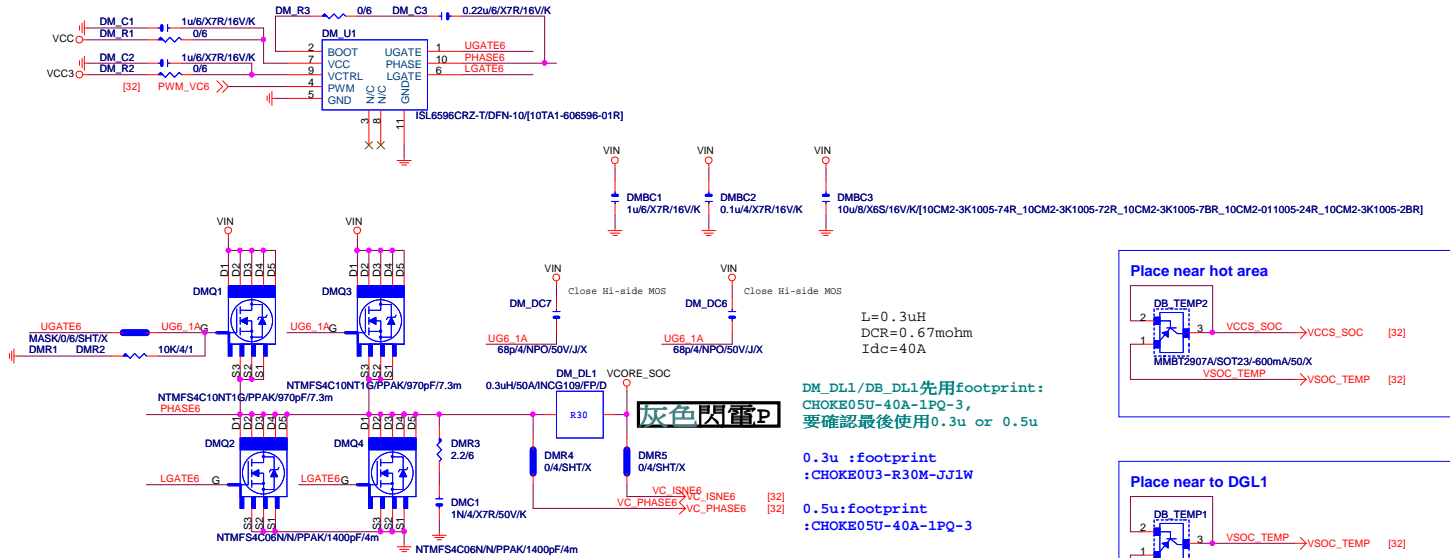


REV:0.1



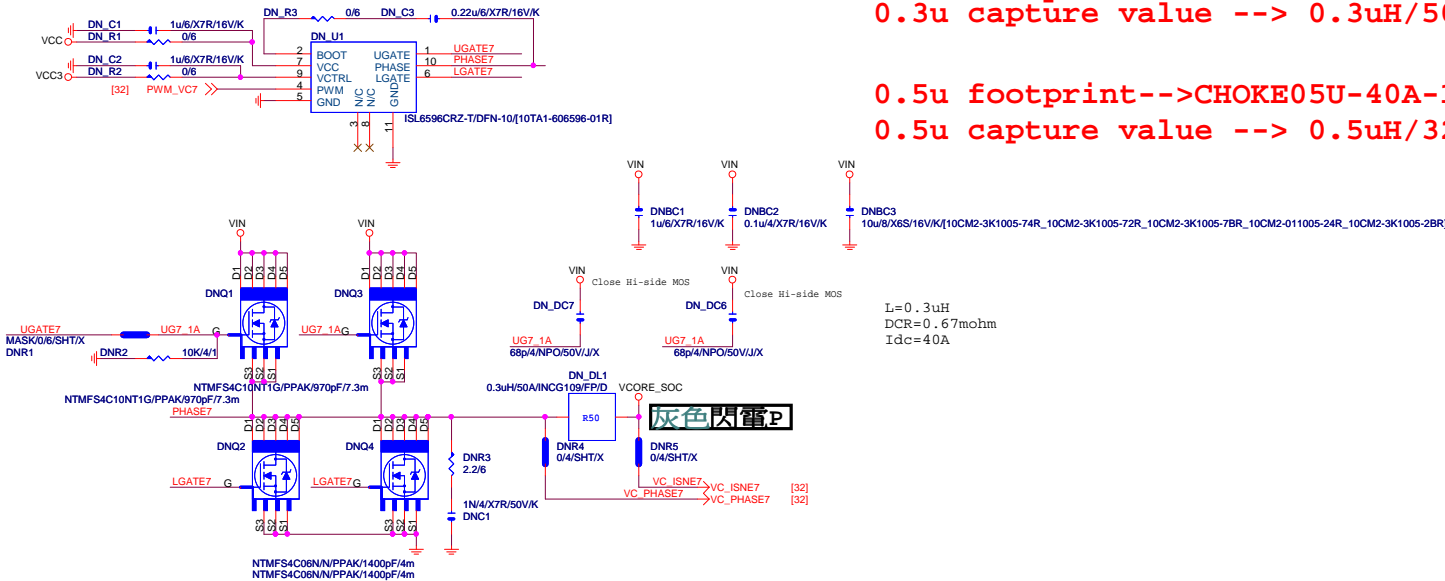
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0.3u footprint-->CHOKE0U3-R30M-JJ1W
0.3u capture value --> 0.3uH/50A/INCG109/FP/D

0.5u footprint-->CHOKE05U-40A-1PQ-3
0.5u capture value --> 0.5uH/32A/INCG109/FSI/D





note:可變更USB NAME



(CLOSE LAU1 PIN22,30,3,8)

LA_VDDIO1

PIN22
LABC2
0.47u/2X5R6.3V/K

PIN30
LABC9
0.1u/4X7R/16V/K

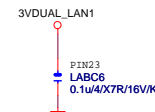
PIN3
LABC3
0.1u/4X7R/16V/K

PIN8
LABC8
0.1u/4X7R/16V/K

LA_VDDIO1

LABC2:1U CLOSE PIN22[REALTEK REQ]

note: lan power連接及電流



(CLOSE LAU1 PIN23)

```
LABC18,27:CLOSE PIN11[REALTEK SURGE]
LABC14,20:CLOSE PIN32[REALTEK SURGE]
```

[illegible]

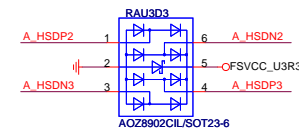
note: lan power連接及電流

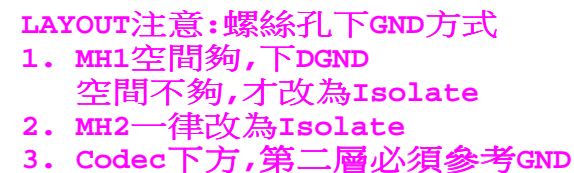
For PVT :LAPW1 改 R0402-2-SHORT20

可變

LAPW1

PS:視EMI需求





<input type="radio"/> MH1	<input type="radio"/> MH2	
DGND	Isolate	

音效區域印刷

GIGABYTE™			
Title Realtek ALC887			
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Rev 4.1

*  → Near MH1

*  → Under Codec

增加 for 實驗雜訊issue , 模組 not yet
用大陸反饋配備 , 底噪小聲, 先移除

*  → Near F_AUDIO

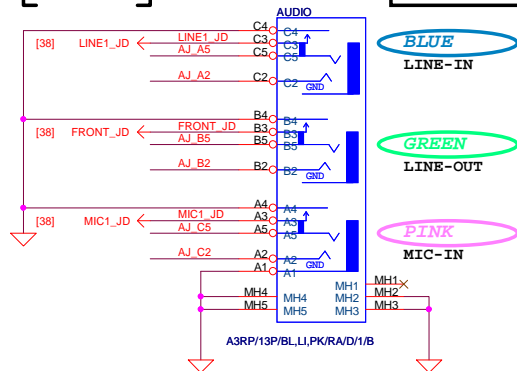
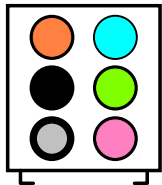
*  → Near Codec

 → Under Audio jack

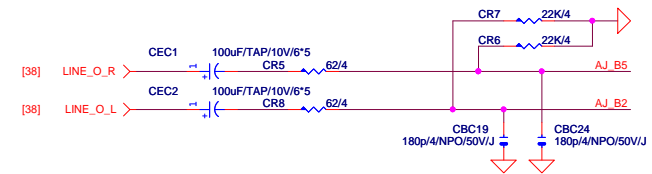
*  → Audio jack - LAN

*量產前,MOATR1/MOATR2/MOATR40ohm改short pad

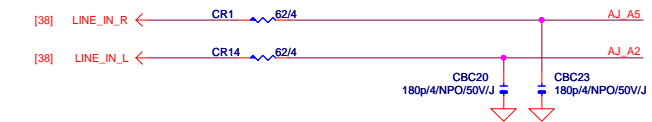
AZALIA JACK



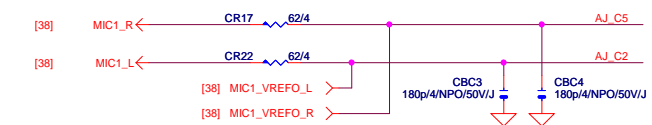
LINE-OUT



LINE-IN



MIC-IN



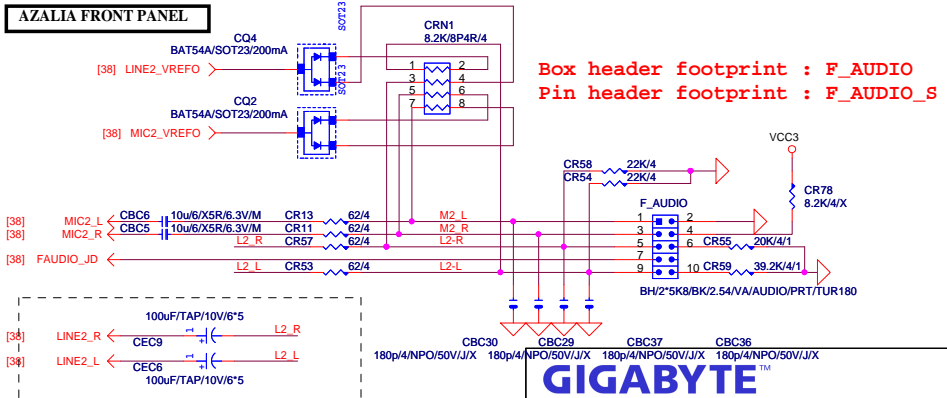
SURROUND

CEN/LFE

SURR BACK

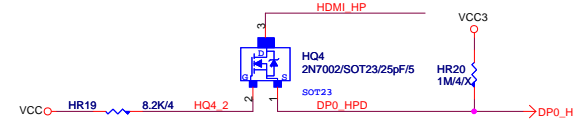
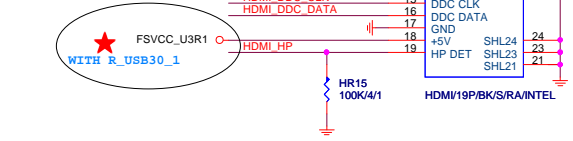
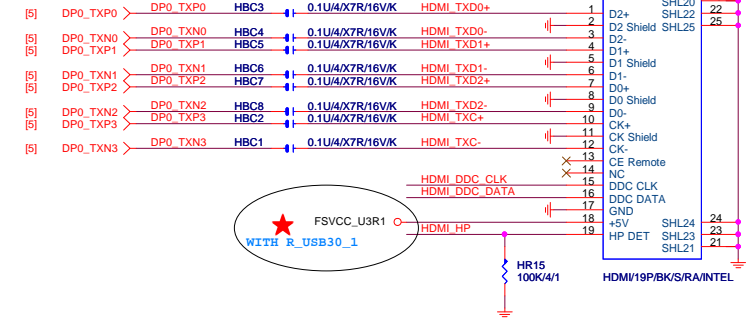
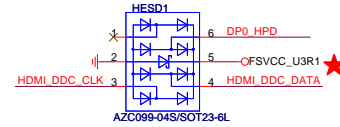
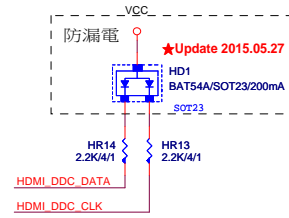
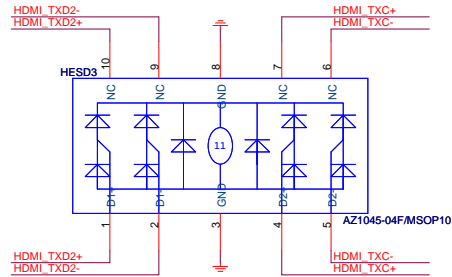
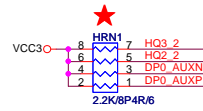
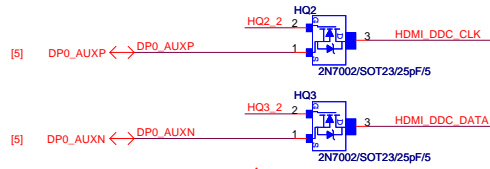
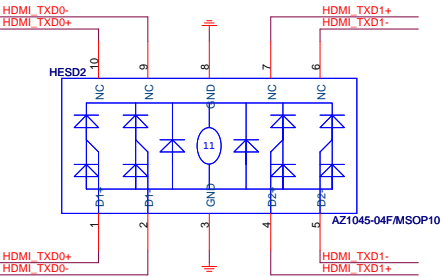
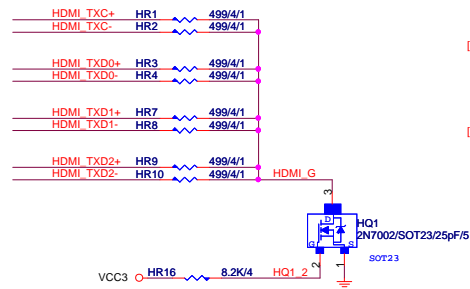
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AZALIA FRONT PANEL

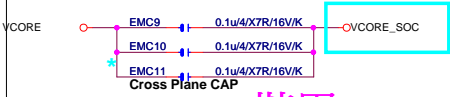
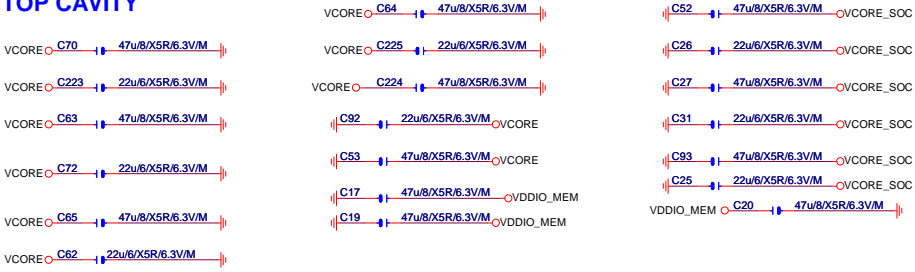


Box header footprint : F_AUDIO
Pin header footprint : F_AUDIO_S

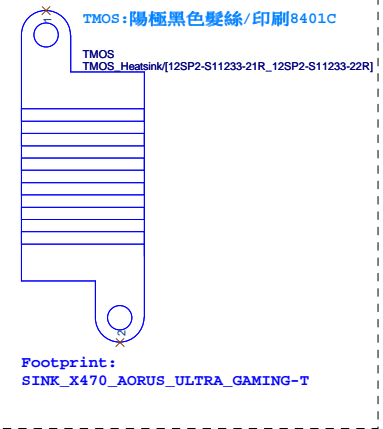
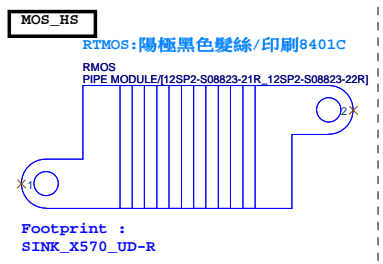
GIGABYTE		
Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	X570 UD	1.0
Date:	Monday, June 24, 2019	Sheet 39 of 47



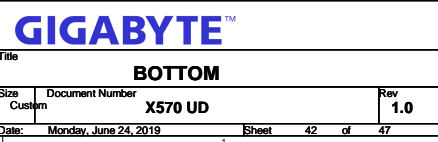
CPU TOP CAVITY

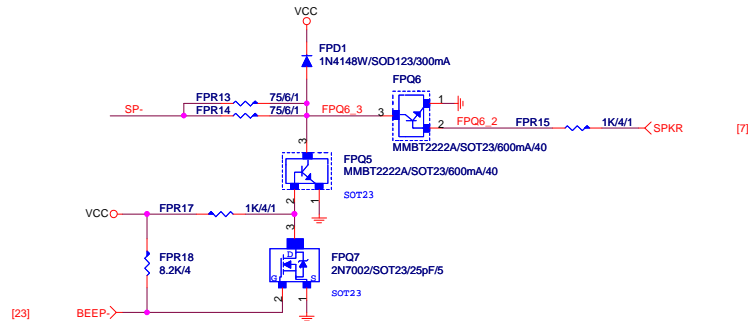
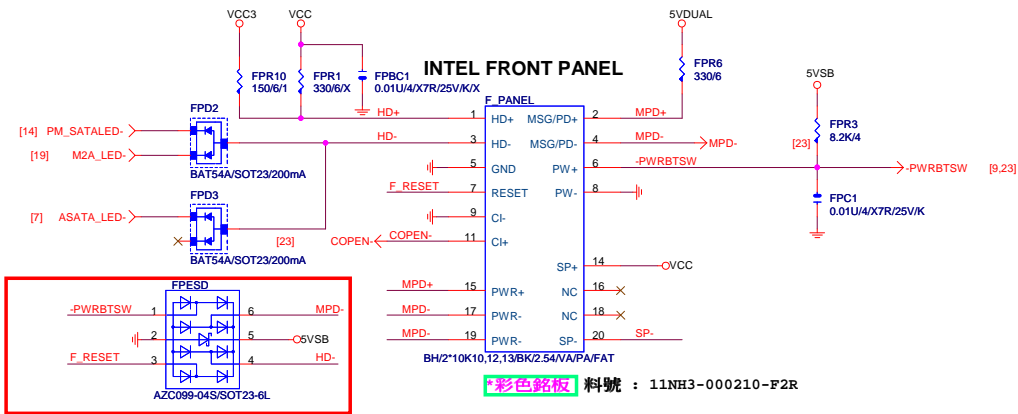


裝甲HEATSINK 分成五大部份



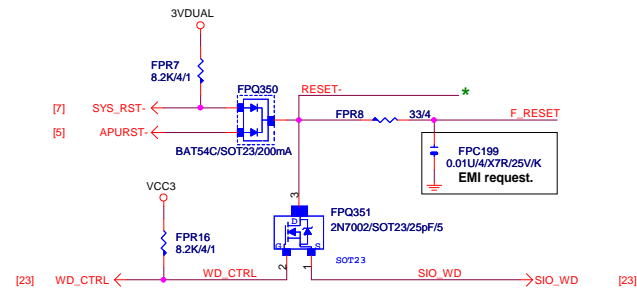
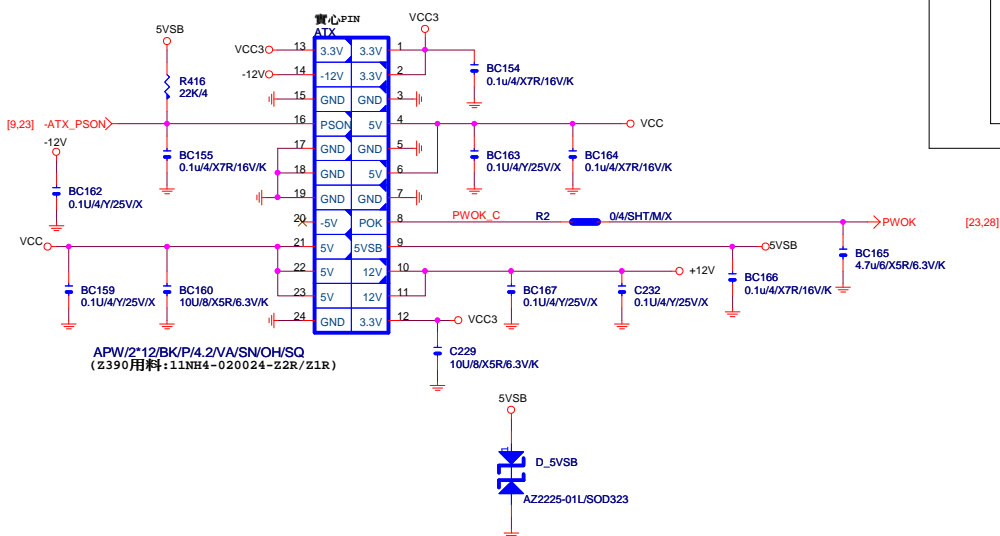
- * PCB顏色 : 咖啡黑
- * 文字面 : 灰色
- * 圖騰 : 待確認ID



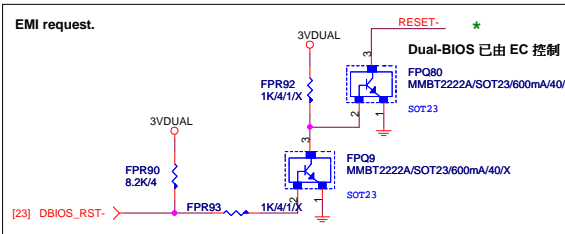


ATX POWER CONNECTOR

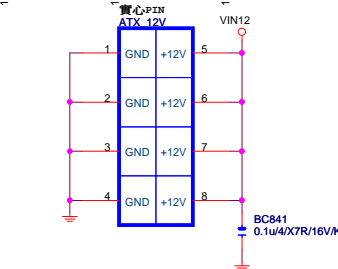
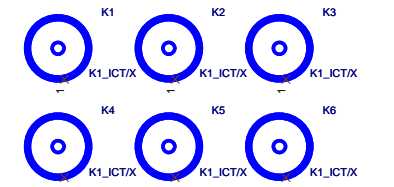
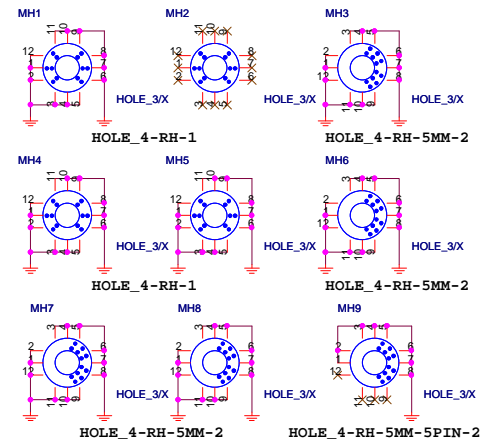
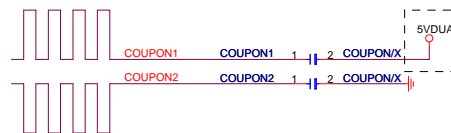
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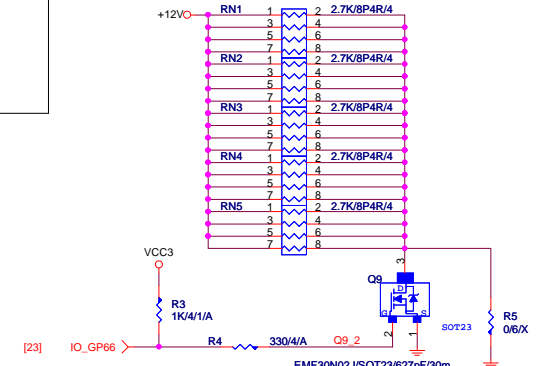
keep-



(靠近ATX CONNECTOR)



APW/2*14/BK/OC/P/4.2/VA/SN/OH/S/PA9T (2390用料: 11NH4-020108-22R/21R)

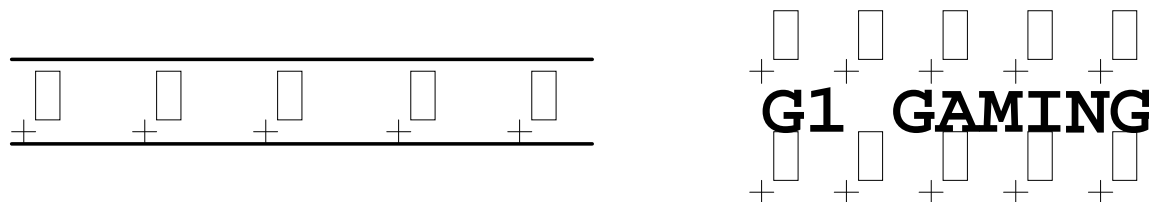


GIGABYTE™			
Title ATX, FRONT PANEL			
Size Custom	Document Number X570 UD	Rev 1.0	
Date: Wednesday, July 03, 2019	Sheet 43	of 47	

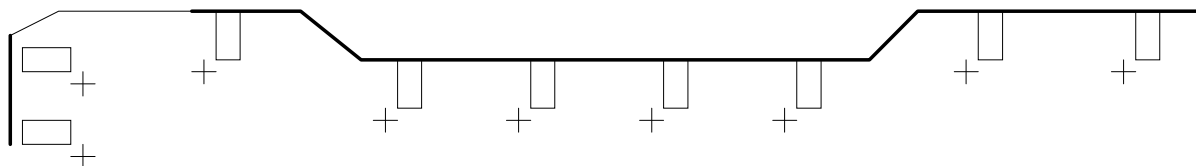
RGB LED LAYOUT 注意事項：

1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
2. 背板 RGB LED 方向整板請統一如下
(整板正極可統一朝下或朝上)
3. 正板 RGB LED 統一方向即可
4. MCU_PW & MCU_PW33電源一律走20mils
5. ECF1,ECF2,ECF3,ECF5 兩端電源走80mils或用鋪銅方式加粗
6. MCU LED 出pin的走線4mils,如:LED_R_1,LED_G_1,LED_B_1
7. LED RGBW rule :W/S=10/5 mils 如:LED_R_11,LED_G_11,LED_B_11..
(包含從晶體到排阻到LED的net)
8. Digital LED NET rule W/S=4/8 mils
GPD0_SDA_B,GPD0_SDA_BB,GPD0_SDA_C,GPD0_SDA_CC

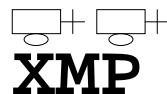
PCB板邊透光model name鏤空+背面 RGB LED



Audio Ground切割線+背面 RGB LED



"XMP"字樣鏤空+背面 RGB測發光 LED

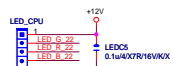


GIGABYTE™			
Title LAYOUT GUIDE			
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第一區 LED

第二區 LED

燈條 LED (LED_CPU放在CPU附近位置)

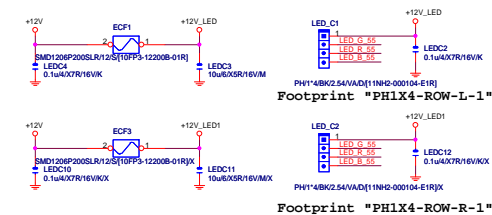


Footprint "PH14-FAN-AMD"

第五區 LED CONTROL

燈條 LED (LED_C1放在PCB左邊板邊位置)

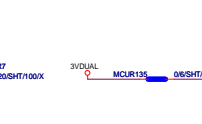
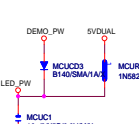
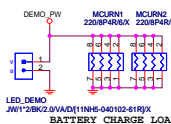
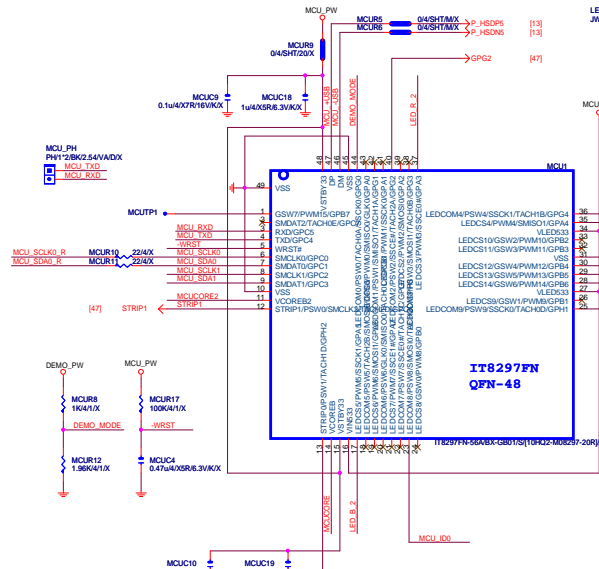
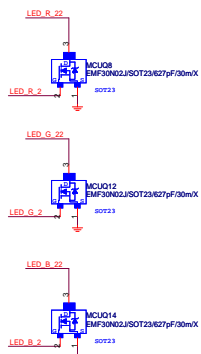
燈條 LED (LED_C2放在PCB右邊板邊位置)



Footprint "PH14-ROW-L-1"

Footprint "PH14-ROW-R-1"

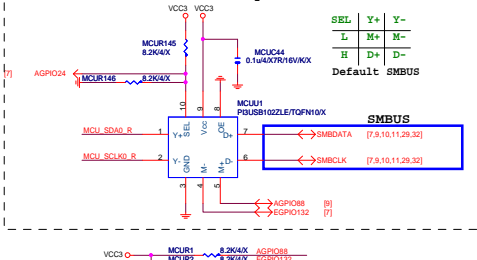
第二區 LED CONTROL



For AMD MCU update

SEL	Y+	Y-
L	M+	M-
H	D+	D-

Default SMBUS



Rev 4.0

第三區 LED

第四區 LED

GIGABYTE™

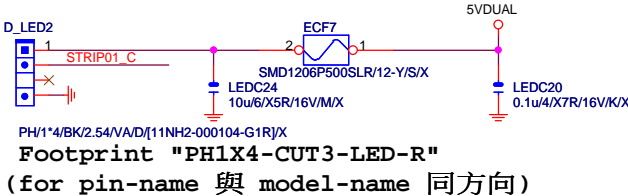
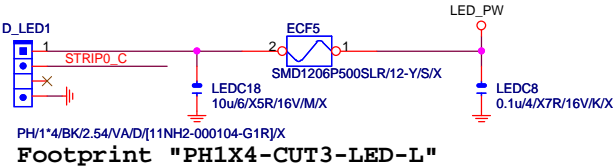
Title		
MODEL / PCB /AUDIO/PCIE LED		
Size	Document Number	Rev
Custom	X570 UD	1.0
Date:	Monday, June 24, 2019	Sheet 46 of 47

第六區 LED (靠近左上板邊位置)

(靠近右下CPU板邊位置)

Digital LED Strip1

Digital LED Strip2



燈條 Level shift

燈條 Level shift

